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3 Dimensional Printed Circuit Board Electroplating Simulation Tools

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Innovation in electronics manufacturing can sometimes come at a dizzying pace. One has only to look at the worldwide proliferation of electronic hardware, especially computers, to realize that modern electronic hardware application often outpaces the technology of its individual components. For instance, circuit board utilization in very sophisticated electronic technologies belies the fact that those very circuit boards are still, in the view of many, electroplated the "old fashioned way".

With the exception of some newer conveyorized copper plating equipment that has focused on HDI manufacturing in Europe and the Far East, significant innovation in copper electroplating of circuit boards has been lacking. Electrodeposition of copper on printed circuit boards has not had a colorful history, especially as the technological sophistication of the boards themselves has so dramatically increased.

This paper addresses an emerging technology aimed at 2 major plating concerns:

- achieving better plating deposit thickness uniformity, especially surface plating uniformity
- achieving through-hole plating uniformity with special consideration given to surface to hole ratio, i.e. surface plating thickness vs. thickness in various locations of the hole

The importance of plating deposit uniformity in circuit board manufacturing touches so many areas: DFM, plating cycle time, material costs, board quality and assembly. Cost issues seem to take a back seat, however, when it comes to getting the product "acceptably" plated and moved to the next printed circuit manufacturing step.

Cost issues are a problem. Deposited metal costs are adversely affected because common overplating wastes metal regardless of whether pattern or panel plating is performed. Because of overplating in the pattern plating process thicker dry film is required and thicker dry film costs the fabricator more. The extra solder mask used to cover overplated areas also increases cost. The plating energy that goes into overplating is lost, not to mention the long plating cycle times that hamper productivity.

Functionally, overplating adversely affects conductor width and thus also affects RF properties of conductor traces. This can be disastrous on some microwave interconnect substrates. Other functional problems from overplating are that modern high-speed electronic circuits, such as those used in computers and communications systems, require controlled impedance lines to maintain signal integrity. Conductor width is one of the parameters that affect the characteristic impedance of the circuit. Controlled impedance lines are often distant from neighboring conductors, while narrow lines and spaces are used in dense circuit areas to facilitate interconnection. This causes problems with plating uniformity.

While it is necessary to form narrow lines in both dense and sparse areas on printed circuit boards, it is a difficult task to control all the processes so that their finished widths are the same. Both etching and other processing parameters, like plating, can affect the uniformity of features between these dense and sparse areas.

Overplating also impacts design and design vs. manufacturability trade-offs are numerous, especially for advanced packages. DFM is stretched to newer limits all the time. It's safe to say that overplating inhibits how far designers can effectively go in creating new interconnect solutions. A subset improvement of DFM could be DFE (design for electroplating). DFE wouldn't be such a tough issue if it weren't for common, non-uniform plating deposit thicknesses, read overplating.

Numerous technology applications aimed at the difficulties in acid copper plating of circuit boards

have been reasonably well documented to date but there are no new developments in plating technology currently used that significantly improve deposit uniformity.

To illustrate, it's not unusual that a plated circuit board with a minimum copper thickness specification of 1.0 mils (usually found near the center of the board) measures well in excess of 2.0 mils elsewhere on the board. It's an accepted fact of circuit board plating life that overplating occurs. Other critical plating issues now manifest themselves in underplating as well. Take the example of underplating in holes (especially underplating in blind via holes) while excess plating occurs on the same board. Overplating and underplating can and do occur on the same circuit board.

Figure 1 is a simple illustration of trace height variations on a circuit board. The overplated areas are usually on the board's perimeter but are not necessarily limited to those areas. Isolated traces and pads not located on the perimeter can still overplate.

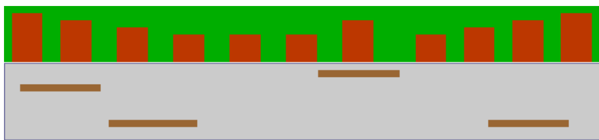


Figure 1

Figure 2 illustrates improvements in plating distribution that result in lower trace height variations.

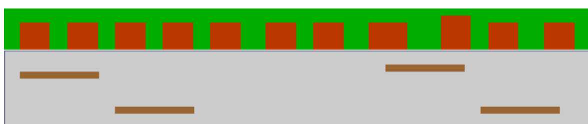


Figure 2

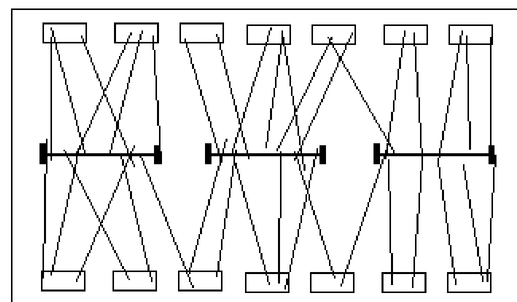
Suffice it to say, the electrode potentials of the complex surface features of a multilayer board have stumped many good engineers. The electrode potentials of circuit features vary across the board's surface. Higher electrode potentials translate into thicker deposits but it's not always easy to determine the overall electrode potential of the board, much less the individual electrode potentials of certain features.

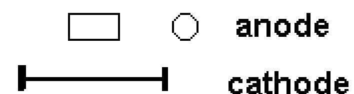
It's understandable how a circuit board perimeter can overplate. One wonders how a small trace area or pad can so significantly overplate. The surface area is small. Theoretically, the kinetics in electroplating on that small an area won't be equal to those of larger exposed copper areas. Underlying surface copper surrounding overplated traces and pads, for instance, plays a significant role. Because it's covered with resist, the underlying surface copper does not plate but it does have electrode potential that affects the exposed copper. The underlying copper surface is directly in the field of plating current flowing from anodes on both sides of the plating tank. The same can hold true for large buried ground plane areas. They have electrode potential but they don't plate. They do, however, subtly affect the electrode potential of surface features that are near them.

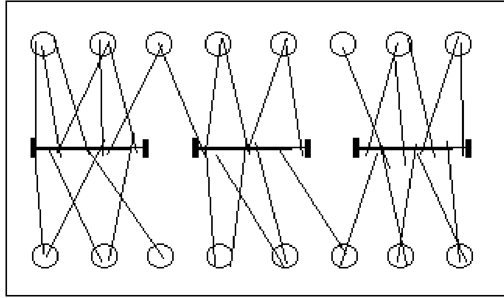
Overall, the result of non-uniform plating, or overplating, is that modern circuit board electrodeposition is carried out at very low current densities, as low as 8 asf, and for long periods of time. This has been a trend since the early 1980's. Fabricators lower the current density, increase the plating time and deal with the overplating (and now underplating too) as best they can.

I recently heard of a 4½ hr. acid copper plating cycle on a complex multilayer board. Now, how does that add to the manufacturing cycle time in a quick turn board shop? Granted, the board had "subs" which contributed to the long time but how or why should we put up with these long plating times and still get such poor metal distribution?

Figure 3 illustrates simple 2 dimensional anode-cathode relationships encountered in electroplating flat substrates.







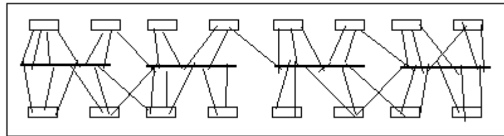


Figure 3

The “view” is that gained from looking down at the top of an electroplating tank. Several anode/cathode arrays are displayed. It becomes clear there are several potential anode cathode relationships that a circuit board might see: wide tanks and narrow tanks, rectangular anodes, round anodes, differing anode to cathode spacing etc. Plating of circuit boards, as in plating of most anything, is confined to the dictates of the electrolyte container – usually rectangular shaped plating tanks with anodes on both sides.

Figure 4 illustrates a 2 dimensional example of simple anode cathode relationships where the current dissolution area at the anode and the plated deposit thickness at the cathode are predicted in a model according to their size, shape, placement in the cell and applied current potential.

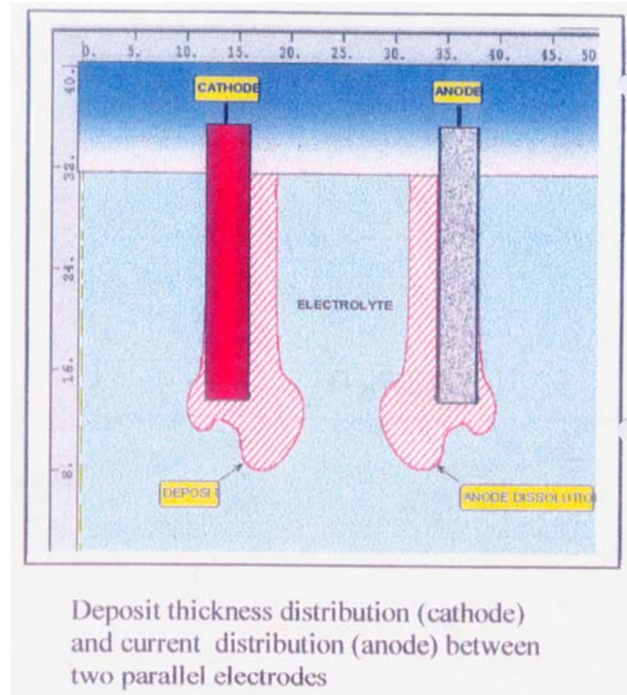


Figure 4

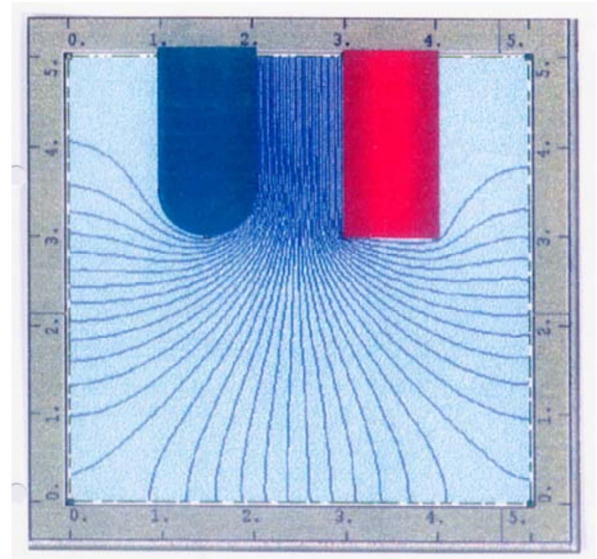


Figure 5

Figures 5 and 6 show the “mapping” of electrode potentials that is possible between parallel electrodes.

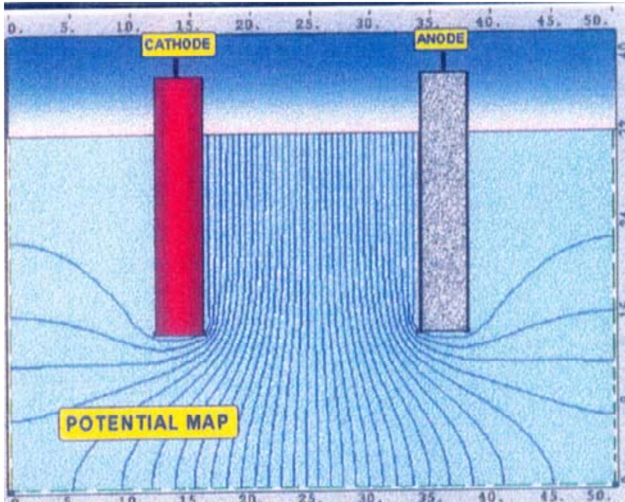


Figure 6

As for electroplating current flow and the behavior of flux lines, as they are called, I have a favorite expression: "the current goes where it wants". It behaves according to numerous electrodeposition laws known in physics and chemistry. Scientists the world over have been experimenting with effects of these laws for years.

Given the size and shape of the electrodes, their distance between each other and the applied current potentials, flux lines can be mapped and understood. Further, their behavior can even be altered by variations in anode/cathode placement. It's also possible, with the use of simple non-conductive barriers placed in the paths of flux lines, to manipulate their behavior. With emerging plating engineering technology that better understands anode/cathode relationships, it's going to be easier for circuit board fabricators to put the plating current where it's wanted vs. where it typically goes in a conventional plating cell.

How can this be accomplished? One of the keys is in understanding the electrode potentials of the circuit board in new ways. For instance, using the information already available about a circuit board from its the design files is an excellent place to start.

The following is usually known before electroplating plating commences:

- surface area of exposed copper on each side of the board
- location of the exposed copper
- surface area of exposed, platable holes

We have great potential to change the way fabricators plate circuit boards by developing the capability to accurately model the plating potential of the circuit board in a useful 3 dimensional model. From such a model it's possible to have accurate information about the behavior of the cell that's never before been available. I know more than one plating process engineer who's been stumped about a problem and fantasized about a scuba dive inside the tank so see "what's really going on in there?" Figure 7 gives us a glimpse, in virtual reality, of just what that scuba dive might reveal. The deposit thicknesses in this 3 dimensional plating model are vividly depicted by color variations.

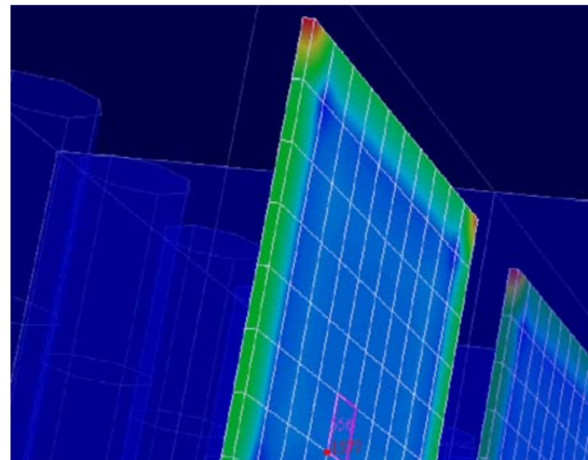


Figure 7

To better understand this plating technology breakthrough let's first take a brief look at some newer copper plating technology advancements that have been employed by fabricators over the last few years:

PLATING Engineering Alternatives:

- Organic Additive Based Systems
- Solution Movement
- Pulse, Pulse/Reverse, WST, CWF Power
- Tank Set-up, Robbing/Thieving, Shields
- Focused, “Designed” Plating

Figure 8

Organic Plating Additives - Organic additive-based system improvements have been developed and tested to improve plating performance, especially throwing power, for over 40 years. The paths leading from the power source to the cathode are made up of several elements that all have some effect on deposition at the cathode.

Figure 9 depicts an electroplating circuit diagram with differentiation of the “electroplating circuit” relationship of the surface to hole.

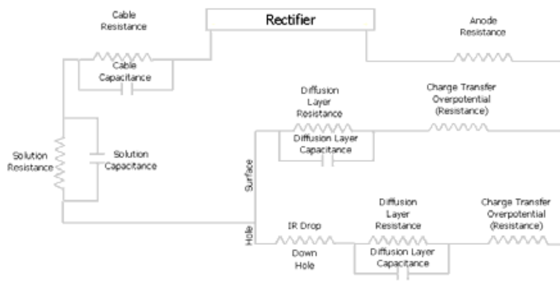


Figure 9

In this illustration the relative importance of the individual elements to each other is not well enough understood to effectively manipulate or control them but they have definitely been considered for research on the effects generated by plating additive or brightener systems. Cable resistance and capacitance, plating solution resistance and capacitance, diffusion layer resistance and capacitance and even charge transfer overpotential are taken into consideration.

Figure 10 is descriptive of an effort to control increases or decreases in resistance due to charge transfer overpotentials as they might be affected by carrier, brightener or leveler additive manipulation in acid copper plating electrolytes. The model leads to manipulation of various organic additive components aimed at improving throwing power.

Charge Transfer overpotential

Hole	$R_{cp(h)} + R_{ct(h)}$ + IR drop
Surface	$R_{cp(s)} + R_{ct(s)}$

Where — R_{cp} = Resistance due to concentration polarization
R_{ct} = Resistance due to charge transfer
IR drop = Resistance due to IR drop down hole (includes solution resistance

Poor T.P.	Hole	20 + 20 +100	140 or 3.5 to 1
	Surface	20 + 20	40
Good T.P.	Hole	30 + 200 + 100	330 or 1.5 to 1
	Surface	30 + 200	230

Carrier and optional levelers increase R_{ct}
Brightener decreases R_{ct}

Figure 10

Organic additive based system improvements have largely been unsuccessful in affecting major changes in plated metal distribution, especially on the board’s surface. Organic additives are almost always necessary to mediate the deposit’s physical properties. Their effect on the cathode diffusion layer is also fairly well understood but there are numerous reasons why strong reliance on organic additives has limitations.

Electroactive organic species chosen for additive use must be strictly manufactured so that they are “pure” and with no organic by-products. It’s been demonstrated that common electroactive species chosen for plating mediation can easily propagate, or grow. What starts as one electroactive organic component can become several separate and identifiable electroactive species after only minimal electrolysis. Coupled with this, leach products from the board and drag over of surfactants (yes, they do get through the rinses) have a definite effect on the overall balance of organic constituents in the bath.

Acid copper electrolytes have accurately been called “organic soup”. Though additives do play a part, their importance and use must be put into proper perspective. They serve an important function. Just don’t rely too much on them because there’s more going on with plating that we just don’t realize yet.

Solution Movement and Impingement – It’s now widely recognized that air agitation in acid copper plating is not necessary. It’s historically been used to agitate the solution enough to adequately

replenish the cathode film at the board's surface. It was once believed that the Holy Grail of plating deposit uniformity would be found in a completely uniform, homogenous diffusion layer thickness over the entire cathode surface and that new types of solution movement might just provide that. It's been elusive, to say the least.

Alternative plating agitation was investigated in the late 70's. Impingement designs aimed at getting more solution into the holes came about in the late 70's and early 80's. Equipment designs were numerous but it was generally concluded that plating solution impingement, Figure 11, created more turbulence difficulties than it was worth and was largely abandoned.

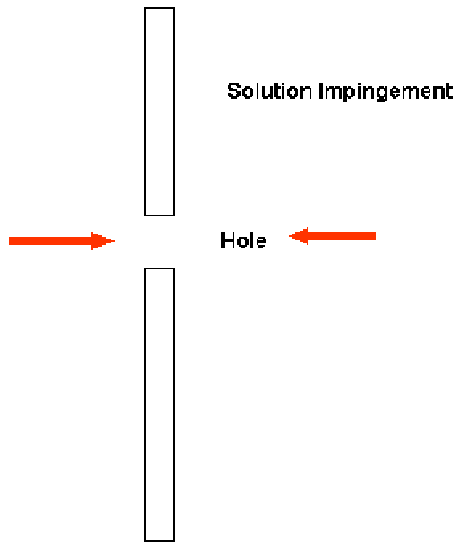


Figure 11

Another form of improved plating solution movement appeared in the 90's: laminar flow solution movement using pumps and solution sparging to direct the solution flow throughout the bulk of the electrolyte.

Ironically the use of modern acid copper plating agitation came about in an effort to counteract plating pits or "mousebites" common in air agitated plating solutions. A welcome by-product was better through-hole plating distribution.

"Airless" acid copper plating of circuit boards was born. The term eductor now almost generically refers to venturi-type nozzles that direct plating solution agitation and flow preferentially throughout the plating tank. For circuit boards, and especially through hole solution movement, it has been found that creating laminar flow of plating solution on both sides of the board results in significant improvements in plating deposit thickness in the hole. The reasons for this are debated but it's really very simple: laminar solution flow that's been properly set up in circuit board plating tanks creates an "airplane wing" effect, or high pressure vs. low pressure.

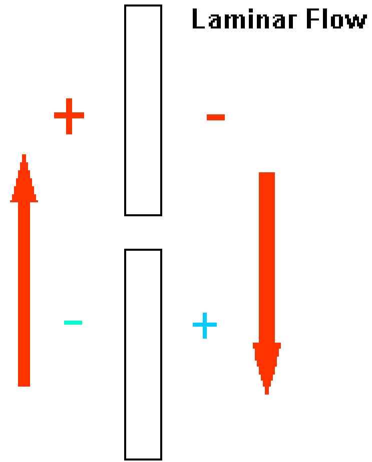


Figure 12

Figure 12 is a simple illustration of laminar solution flow. The solution flow characteristics created by good laminar flow on both sides of the board, as practiced today, are not really constant and their flow pressures are not always equal. Therefore, when there are small but constant flow rate variations on either side of the board there is better exchange of fresh, copper-rich plating solution through the holes. The solution moves better from side to side through the hole.

When this occurs, plating deposit thickness improves in the hole because copper ions are more rapidly replaced. Contrary to some old beliefs, the holes of circuit boards are <u>not</u> low current density areas. The principle reason that copper deposits are thinner in the holes, often resulting in "dog-boning", is simply that the holes have become starved for copper ions.

Plating Current - Pulse/Pulse Reverse Power, Complex Wave Form – The industry is looking to the power supplied in the copper electroplating process to find improvements and well it should. Wave switching technology power supplies showed us the way to cleaner power output. Pulse/pulse reverse and CWF power is showing some promise.

The fabrication industry has fretted over characterizing the duty cycles in pulse/pulse reverse power transmission to match the plating characteristics of certain board designs. This has been an obstacle but some progress has resulted. The capital expense of new power has also held some fabricators back.

Something more basic is lacking in the plating circuit boards:

- The capability to selectively focus plating current where it's needed and/or to inhibit or shield plating current from areas where circuit boards overplate.

Plating Equipment Tank Set-Up, Plating Current Robbing or Thieving

Optimizing the plating equipment set-up is an obvious place to start improving plating deposit thickness distribution. Changes in anode cathode relationships, including size, number and location of anodes, have been employed in electroplating all manner of substrates for several decades. There's no question that manipulations of the anodes and cathodes can profoundly affect the electroplating deposit uniformity on circuit boards and all plated substrates for that matter.

Figure 13 represents an example of the deposit thicknesses commonly seen on circuit boards. The plating thickness excesses are generally tolerated.

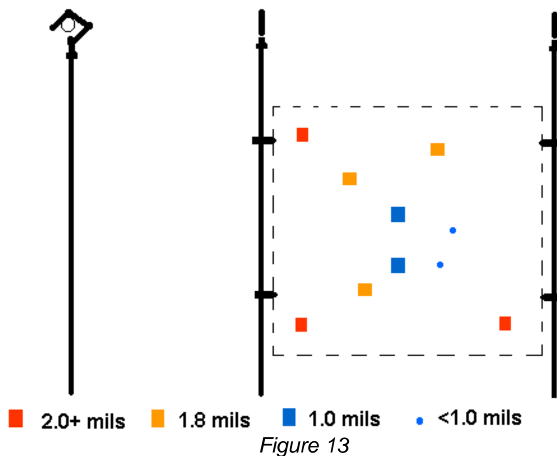


Figure 13

Plating current robbing or thieving is often an adjunct to optimizing the set-up of plating equipment. Figure 14 represents an electrode potential modification to the circuit board cathode where raw, conductive laminate strips are placed on a rack to "thieve" plating current from the board.

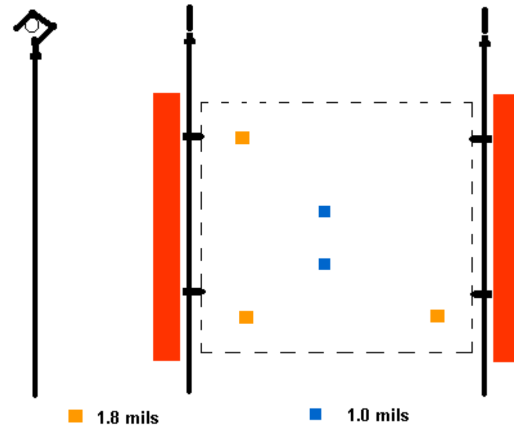


Figure 14

The effect tends to spread out the current distribution, in some cases just enough, to improve deposit uniformity. From non-acceptable to acceptable can sometimes be as little as reducing overplating from a 2.2 mils deposit thickness to 1.8 mils. No pun, there's often a fine line between good and bad plating thickness distribution.

Figure 15 represents the familiar current thieving that's designed directly into the board.

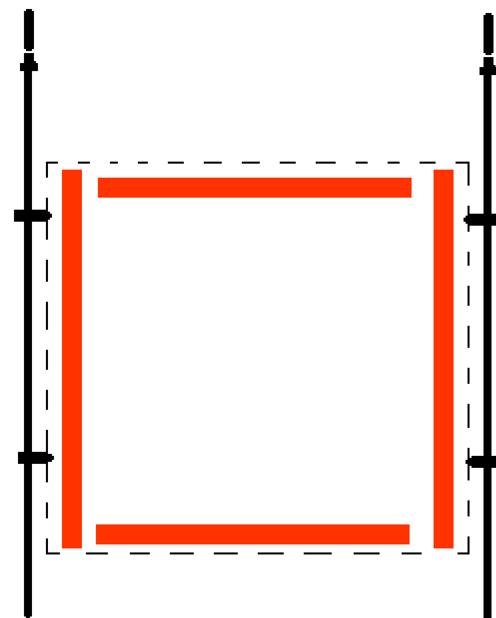


Figure 15

Thieving can be large exposed copper areas, dot patterns or even exposed copper strips. With some designs circuit fabricators even use copper thieving

tape. They manually apply the tape to specific areas of the board before electroplating.

Focused or Designed Plating - There's just one problem with trying to optimize the set-up of anode cathode relationships and experimenting with current thieving: it's tedious, time consuming and is largely done by trial and error. Most plating department engineers have little time for it because they see little or no significant improvement resulting from their countless hours of work.

Picture the trial and error part of trying to better focus the plating current, assuming the engineer has a good idea where to start: The equipment is "optimized", circuit boards are plated, thickness measurements are taken, sections made and evaluations documented etc. If the plating results aren't acceptable, what is an engineer to do?

- Move anodes a little this way or that?
- Add a few anodes?
- Remove a few anodes?
- Put thieves on the rack?
- How large do the thieves need to be?
- Where should they be placed to have the optimum effect on plating results?
- How would plating in a different tank set-up work?

The list goes on and on. The realities of production plating impose limits on time available for this type of testing. Plating engineers and plating line personnel rely on a combination of many years of experience and gut plating instinct combined with quality department acceptance, sometimes grudgingly, to produce acceptable plated boards. The plated metal distribution is something less than uniform but the trade-offs in manufacturability generally dictate acceptance of the results.

A new way to better focus plating current is to optimize tank design and set-up with plating engineering software expressly made for that purpose. Sophisticated technology that's production proven and currently used for electroplating engineering in other manufacturing industries makes it possible for circuit board fabricators to dramatically improve the way they plate boards.

Let's revisit the plating tank "scuba dive".

Figure 16 depicts the 3 dimensional modeling of a circuit board plating tank in a shop where there are several tanks but with 2 differing plating tank set-ups: one with anodes parallel to the side of the tank and the other (Figure 17) with anodes perpendicular to the side of the tank.

The model has been set-up with an electrochemical data base of the plating bath characteristics, in this case acid copper, the desired plating time and desired current density. The boards are 18X24, plated in 3 dimensional simulation with acid copper at 15 asf for 90 minutes.

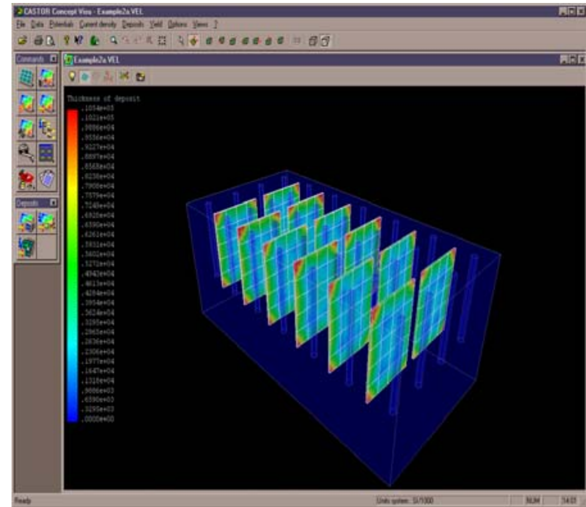


Figure 16

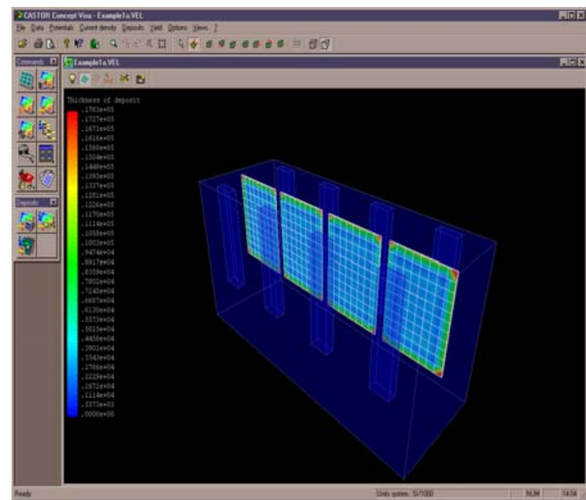


Figure 17

Any electrolyte can be characterized for this model but acid copper is the main concern here. Acid copper deposits are typically the thickest and therefore the most overplated and wasted. The engineer working with this model can now make an intelligent choice about which plating tank to use.

This electroplating engineering technology, used on a standard PC, enables the plating engineer to accurately plate these boards in simulation and then use the information as a guide to setting up real life plating. There's no question that, given the choice, the operator should plate these boards in the tank set-up that overplates the least.

A unique feature demonstrating the sophistication of this plating engineering tool is that the plating simulation can display the modeled plating thickness in colors. Red is the thickest deposit and blue is the thinnest. The relative thickness values can be ascertained on the color scale that accompanies the simulation. Another feature of this simulation is that the total weight of deposited metal can be calculated for each board plated. An obvious use of this feature would be to predict metal usage and then be better able to understand plated copper material costs, per board. This degree of understanding the plating process has not possible before now.

Figure 18 demonstrates another engineering use for accurate plating simulation: the capability to understand current density distribution on the anodes and cathodes.

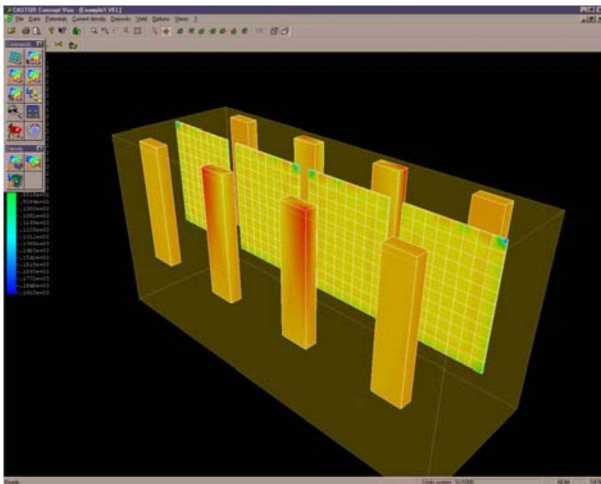


Figure 18

In this illustration, the current densities are also displayed in colors (the colors are different from the color scale of the plating deposits simulated earlier). Take special note of the current density potential of the 2 center anodes. These anodes will not behave the same as the ones on the ends of the tank. As Jack Winters alluded to in his article "The Anodes Side of the Story", this can have a dramatic effect on deposition at the cathode.

Another means to focus plating current is the use of shields. Plating current takes the path of least resistance and if it is forced to go around a shield, its deposition power and strength is diminished. As pointed out in the graphics of plating current flux line mapping earlier, there are definite relationships between anodes and cathodes that result in current flow that can be controlled by interposing shields in the path of the current flowing throughout the cell.

Some of the automatic equipment available today has employed the use of shields that directly protect the bottom of the board. These shields have a stabilizing effect on the racking of the boards and can be configured to protect the bottom of a variety of sizes (depths) of boards from burning or overplating. This is important because anodes in a plating tank are usually a fixed size and shape but the board dimensions and their electrode potentials vary. Some boards will burn much more readily than others.

Figure 19 is an example of a common, a non-conductive plastic shield that is perforated and placed between the anodes and cathodes.

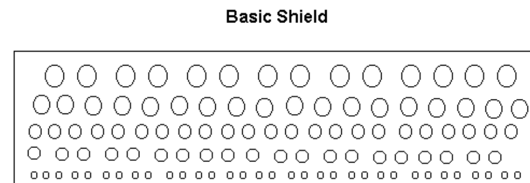


Figure 19

Figure 20 depicts how the perforated shield might be placed in a plating tank to redirect current flow. Burning and or overplating near the bottom of the boards is controlled by allowing the passage of less current to that area than to the middle and upper portions of the boards.

Both perforated shields and bottom shields are shields in a general sense only. They don't permit specific focusing of the plating current so much as they block overplating and/or inhibit burning on specific areas of the boards.

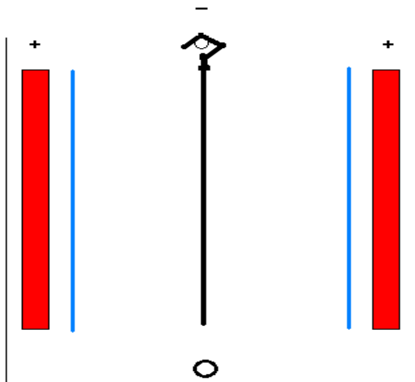


Figure 20

Using a slightly different example for printed circuit board plating shields, my intuition tells me that a plating shield to focus plating current on specific areas of the board, say an array of blind via holes, might look like something like the shield set-up in Figures 21 and 22.

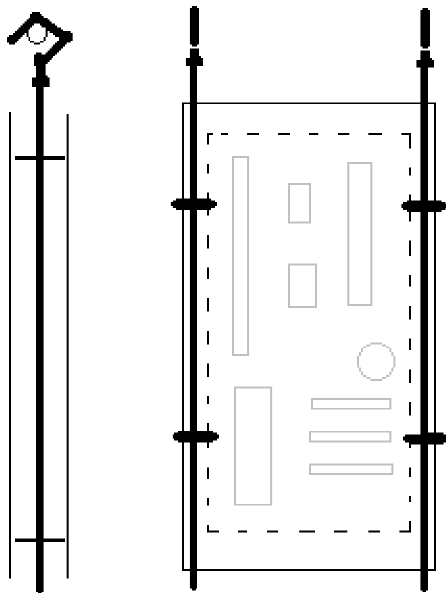


Figure 21

There is a side view of a rack/shield configuration and a front view depicting the position of the shield. The dotted line represents the position of the circuit board. Shields are placed either on both sides of the rack or attached to both sides of the board using the tooling holes as fixtureing aids.

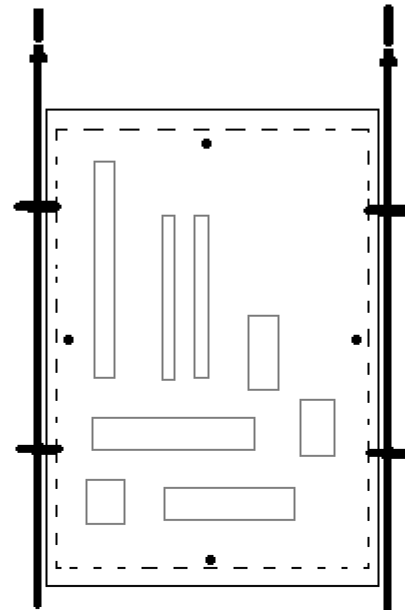


Figure 22

Plating current (remember the flux lines?) directly passes through perforations in the shield but is blocked or shielded from areas that typically overplate. The plating current potential re-directed by the shield is diminished once it finally reaches the cathode and plating thickness uniformity is improved.

I've learned 2 things from these examples: plating set-up and optimization is NOT intuitive and neither is the prospect of accurate plating shield design. Optimization requires complete understanding of the electrode potentials of the cathodes and anodes together.

Figure 23 depicts a plating shield design that was suggested not by intuition but after using the 3 dimensional plating simulation tool referred to above. The shield opening isn't anything like what intuition suggested earlier.

Emerging plating technology software is enabling the electroplating engineer to approach the plating process with a high level of understanding just what the final results will be. This technology enables pre-engineering for plating set-up, whether that entails the use of robbers and thieves, the optimum placement of cathodes and anodes or even which

tank set-up would be best for an engineer to choose in plating a critical job.

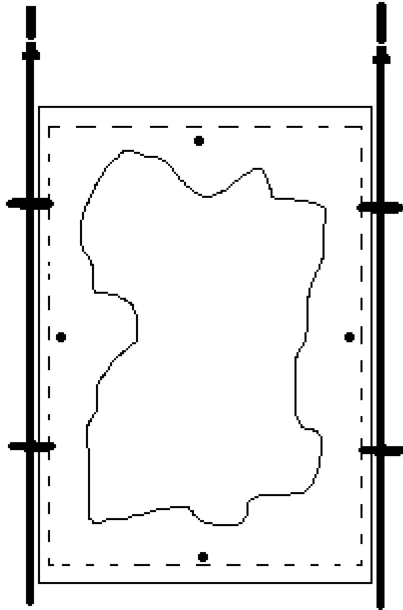


Figure 23

To understand the origins of such sophisticated engineering software it would be helpful to review industrial plating applications that have similar plating problems, namely overplating and underplating. Figure 24 depicts an industrial plating tank simulation.

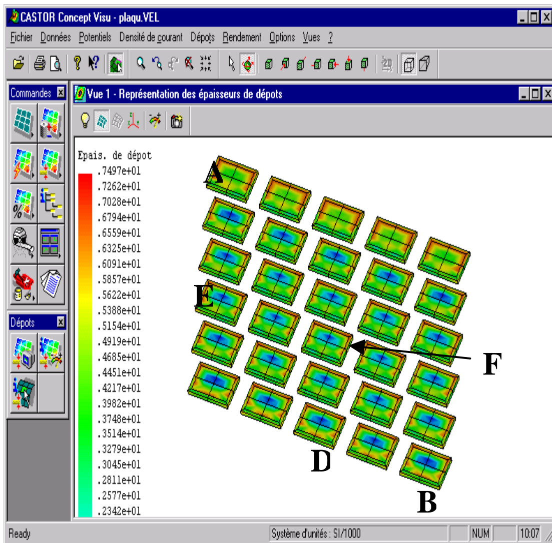


Figure 24

In this case, flat plating fixtures that hold many smaller parts are electroplated. The engineering of plating equipment with 3 dimensional plating simulation in this example enabled complete engineering and design of the plating line before any substrates were ever plated. The goal was to plate the fixtures uniformly. If the fixtures plate uniformly, so also would the parts they contain.

How accurate is plating simulation? Figure 25 shows important relevant data of the simulation vs. the actual deposits after this plating line was run in actual production.

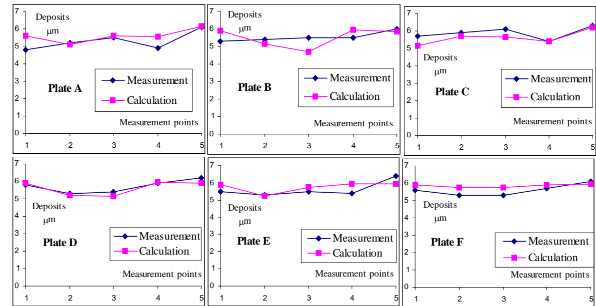


Figure 25

There is insignificant variation in the simulated and actual plated deposits and 95% simulation accuracy can be achieved.

Other examples of 3 dimensional plating simulations further encourage the use of such technology for plating circuit boards.

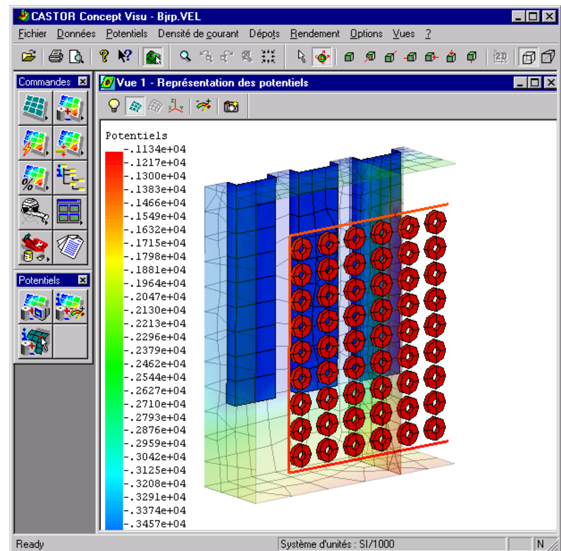


Figure 26A

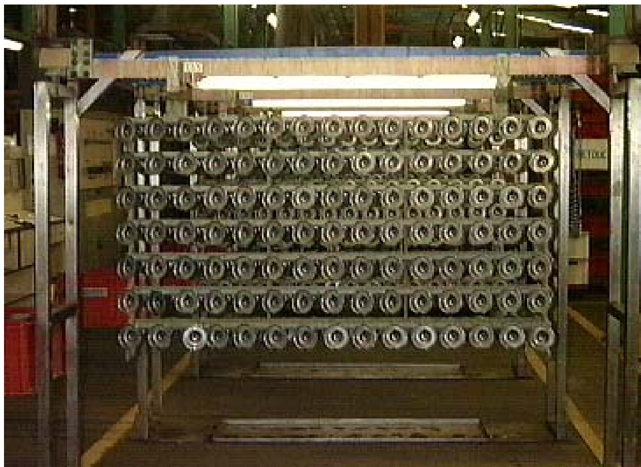
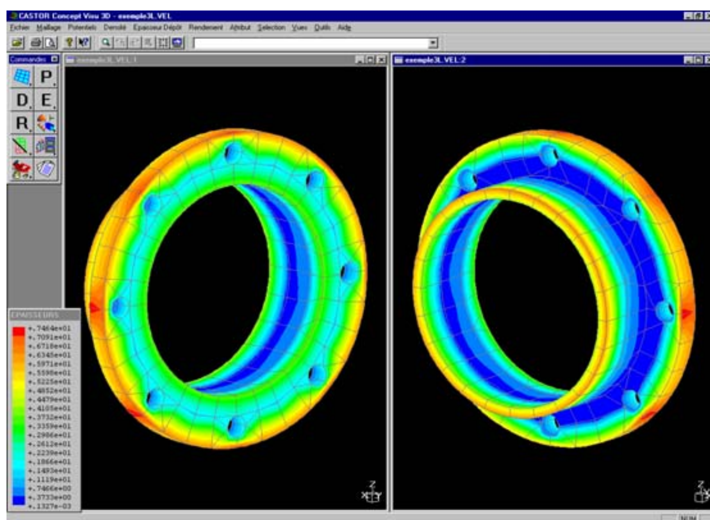


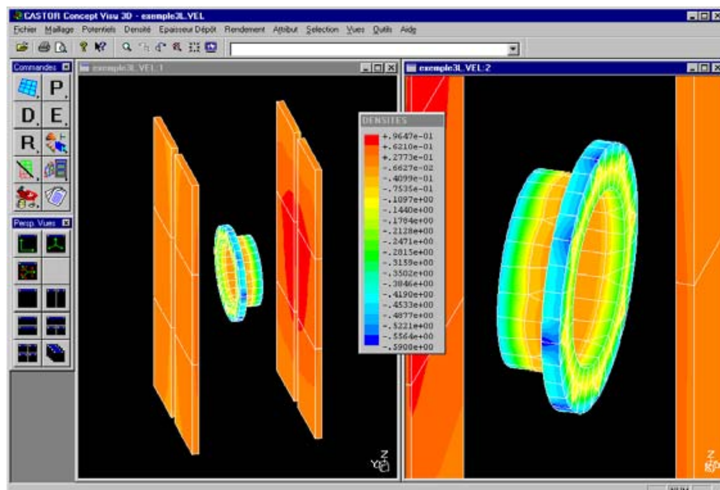
Figure 26 B

Figure 26A depicts a model developed by a plating engineer to optimize racking in conjunction with different anode shapes and placement. A photo of the real parts is seen in Fig 26B.

Figures 27 and 28 give important detail on the plating of an individual component part.



Figures 27 and 28



Notice the detail of the deposition thicknesses, Fig, 27, and in particular, the anode “hot spot” in Fig 28 model. This is important information for the plating engineer.

The implications for improving the deposit uniformity in plating printed circuit boards are enormous. Cycle time reduction first comes to mind. If the plating current is properly focused, the minimum plating thickness specification will be achieved much earlier in the plating cycle.

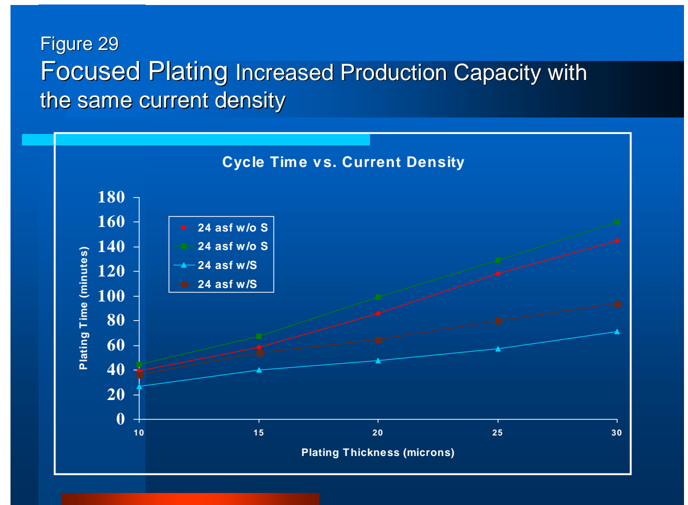


Figure 29

Figure 29 represents an illustration of cycle time reduction made possible by better plating distribution. The example compares regular tank set-up vs. the use of plating shields to focus plating current. Such optimization is not possible without embracing new plating engineering technology.

Other considerations for plating deposit uniformity, as mentioned earlier, are material cost reductions. Figures 30, 31 and 32 depict copper, solder mask and dry film savings possible with better plating distribution.

Figures 33 and 34 represent summaries of these savings for shops producing 500 and 1600 panels/day respectively.

Quality improvement implications of improved plating deposit uniformity continue being investigated and will be the subject of further studies.

Figure 30
Cost Benefits of Improved Plating Deposit Uniformity

- Improved cost efficiency from
  - Solder mask savings
  - Copper metal savings
  - Dry Film Savings

Figure 31 Savings - Soldermask

- Plating test (Pattern Plating)
  - Conventional Plating 24 - 56µm
  - Optimized Plating 24 - 30 µm
- *15% Savings in Soldermask*

Figure 32
Savings - Copper Metal

- Improved Plating Distribution
  - Conventional Plating - 70% Distribution
  - Optimized Plating - 95% Distribution
- *25% Savings in copper metal*

Figure 33
Savings – Dry Film

- Reduced Dry Film Thickness specs.
  - Conventional Plating – 2.0 mil DF
  - Optimized Plating – 1.6 mil DF
- *20% Savings in DRY FILM*

Figure 34
Overall Raw MaterialSavings

- 1600 Panel/day production
- 1 panel (18" x 24") is 6 ssft
- 2,400,000 ssft per year

- 15% Soldermask savings
  - Based on 0.20 US$/ssft
  - *72,000 US$ per year*
- 25% Copper Savings
  - Based on 2.0 US$/KG
  - *31,250 US$ per year*
- 20% Dry Film Savings
  - Based on 0.20 US$/ssft
  - *96,000 US$ per year*

Total = $199,250 (US) per year

Figure 35
Overall Raw Material Savings

- 500 Panel/day production
- 1 panel (18" x 24") is 6 ssft
- 750,000ssft per year

- 15% Soldermask savings
  - Based on 0.20 US$/ssft
  - *22,500 US$ per year*
- 25% Copper Savings
  - Based on 2.0 US$/KG
  - *9,765 US$ per year*
- 20% Dry Film Savings
  - Based on 0.20 US$/ssft
  - *30,000 US$ per year*

Total = $62,265 (US) per year

Figure 36 **Conclusions**

Future printed circuit board plating technology can lead to additional utilization of printed circuit CAD data. When combined with 3D modeling of plating tanks and fixtures, accurate simulation without time-consuming trial and error plating can occur. Focused plating current will significantly improve plating deposit uniformity resulting in:

- **Reduced metal usage and raw material costs (Cu, SM, DF)**
- **Plating Time Cycle Reduction**
- **Significant improvement in plated board QUALITY**

Conclusions

The future of printed circuit board plating technology leads to effective interpretation of printed circuit CAD data that, when combined with 3D modeling of plating tanks and fixtures, accurately simulates plating without time-consuming trial and error. Effective plating engineering simulation leads to focused plating current that will significantly improve plating deposit uniformity. This will result in reduced material costs, reduced cycle time and improved board quality.

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