

# A Performance Simulation Tool for Bipolar Pulsed PCB Plating

Gert Nelissen; Bart Van den Bossche, Luc Wanten  
ElSyCa N.V., Kranenberg 6, 1731 Zellik, Belgium

Presented to IPC in Anaheim, CA 2005 by  
Roger Mouton, EIMC Advanced Plating Technologies

## Abstract

The copper plating process is one of the most critical steps in the high end PCB manufacturing process. Although the deposition inside through holes and blind holes is a key factor for reducing the fall out fraction, the thickness distribution over the entire layout is also critical, in particular for multiplayer designs. A performance plating simulation tool (P2ST) for the prediction of deposit thickness distribution over PCBs is presented. This tool takes into account the bath characteristics (conductivity, electrode polarization), the PCB layout, the electrical signal parameters (DC current or bipolar current amplitudes and duty cycle), and the PCB positioning in the plating tank.

P2ST allows the process engineer to perform a fast prediction of the deposit thickness distribution over tracks, pads, ground planes, robbers, etc. The P2ST tool can be used by any PCB manufacturer either in the cost estimation phase and/or as an auxiliary tool in the CAM work flow area. In the latter case, P2ST represents a powerful asset for the optimization of the pulsed signal and/or background patterns (copper balancing) towards deposit uniformity specifications.

## Introduction

Simulating current density and deposit thickness distributions in electrochemical plating tanks has become common practice. Most simulations are based on Laplace-type models that take into account:

- plating tank configuration
- configuration of the work piece or substrate to be plated
- presence and position of screens, current thieves and auxiliary anodes
- ohmic drop effects in the electrolyte (depending on electrolyte conductivity)
- linear or non-linear polarization/current density relations at the electrodes
- injected current (DC or pulsed) through the anodes

The validity and accuracy of these Laplace-type models depends on the rate of stirring or electrolyte refreshment in the reactor (compared to the range of applied current densities), enabling the process to overcome metal ion mass transfer problems. The acid copper plating bath characteristics (cathodic and anodic polarization behavior) can, for example, be measured with a Rotating Disc Electrode (RDE).

The result of these simulations is basically a graphic understanding of current density distribution  $j$  over the electrodes. The layer thickness distribution  $d$  on the cathodes is easily obtained using Faraday's law:

$$\Delta d = \frac{M \Delta t j}{\rho z F},$$

assuming a 100 % efficiency for the deposition process.  $M$  holds for the atomic weight of the metal,  $\rho$  for the density,  $z$  is the number of electrons exchanged in the metal deposition reaction, and  $F$  is Faraday's constant.

Most literature publications deal with simplified two dimensional (2D) cross sections of a plating tank for simulation proposes, only a few papers deal with full three dimensional (3D) current density distribution and layer thickness simulations, for example [1, 2].

## Modeling PCB plating processes

Modeling PCB or wafer plating processes poses some additional difficulties, since the patterned electrode surface is to be accounted for. Moreover, 2D cross sections are irrelevant in this case and a full 3D approach is required.

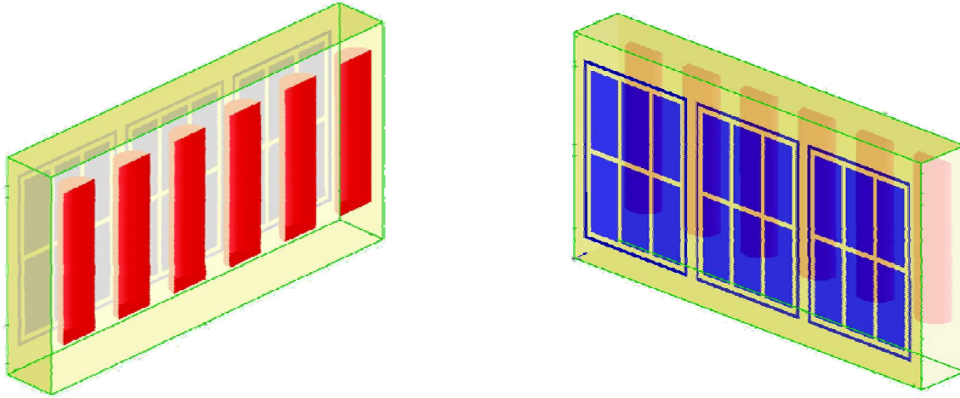


Figure 1: vertical plating tank configuration with anode baskets (red) and PCB's (blue)

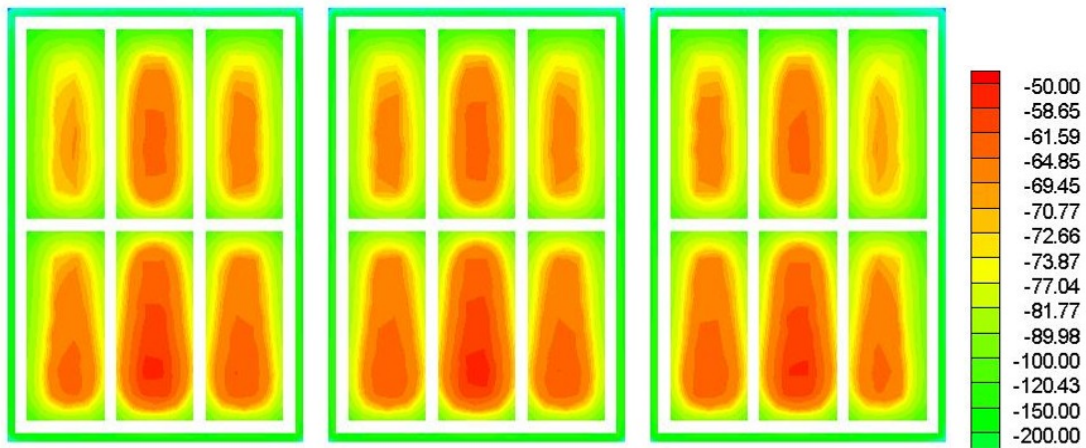


Figure 2: current density distribution (in  $A/m^2$ ) over the PCB surfaces under normal operating

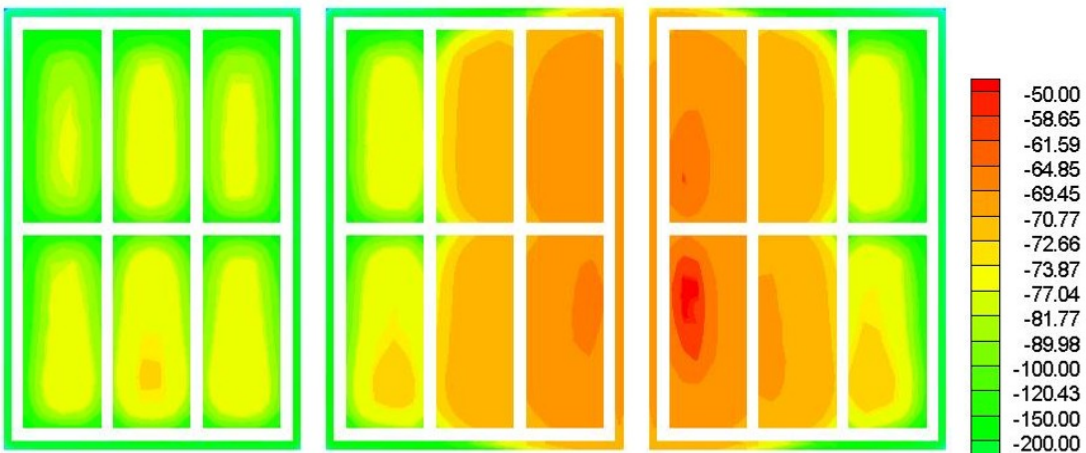


Figure 3: current density distribution (in  $A/m^2$ ) over the PCB surfaces with two anode baskets empty

For vertical PCB plating processes (Figure 1), a distinction can be made between reactor (plating tank) scale simulations (macro scale), PCB/pattern scale simulations (meso scale) and feature scale simulations (micro scale). Macro scale simulations predict the difference in layer thickness from one board to another, or from one printed circuit pattern to another on the same board. An example of the macro scale current density distribution is given in Figure 2 for normal operating conditions and for an anomalous situation with 2 empty anode baskets in Figure 3. Note that the influence of the circuit layout has not been taken into account. Meso scale simulations however incorporate the printed circuit layout, since the layout is determinant for the distribution of electro-active zones on the board. An example of a typical printed circuit layout is given in Figure 4. Calculations for an acid copper DC process based on the numerical model presented in [1] have been performed. Figure 5 shows the corresponding current density distribution, with the blue color corresponding to high (cathodic) current densities. Clearly, the edge effects on the electroactive surfaces are visible. The red zones correspond to the masked area.

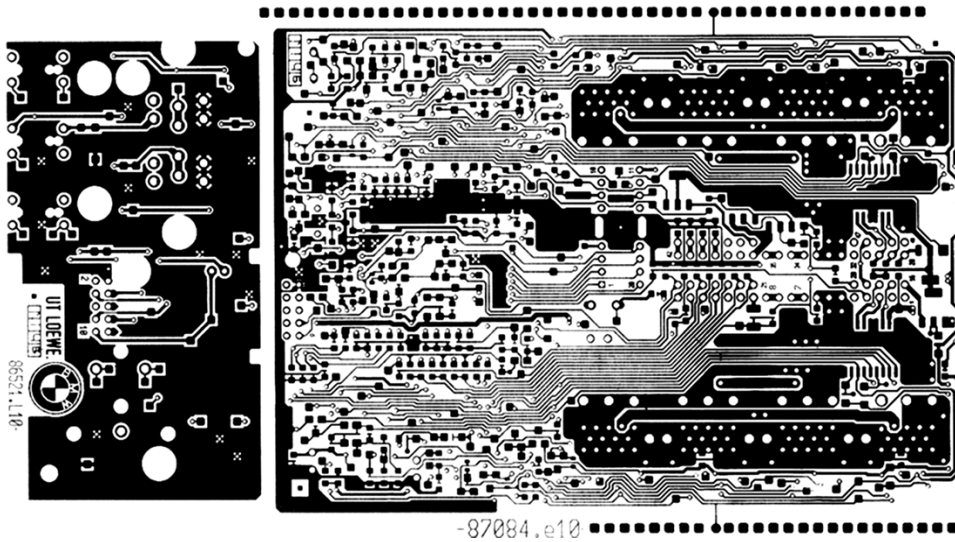


Figure 4: typical printed circuit layout

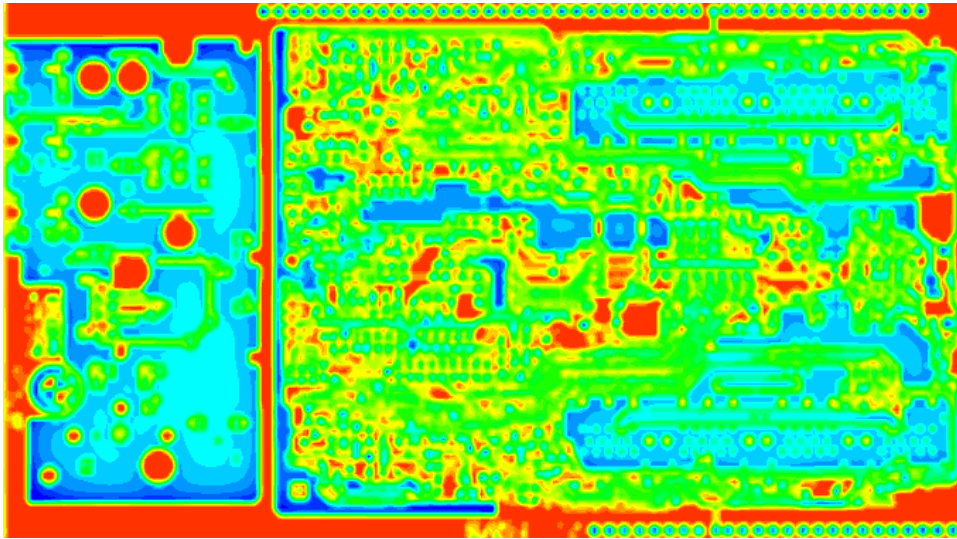
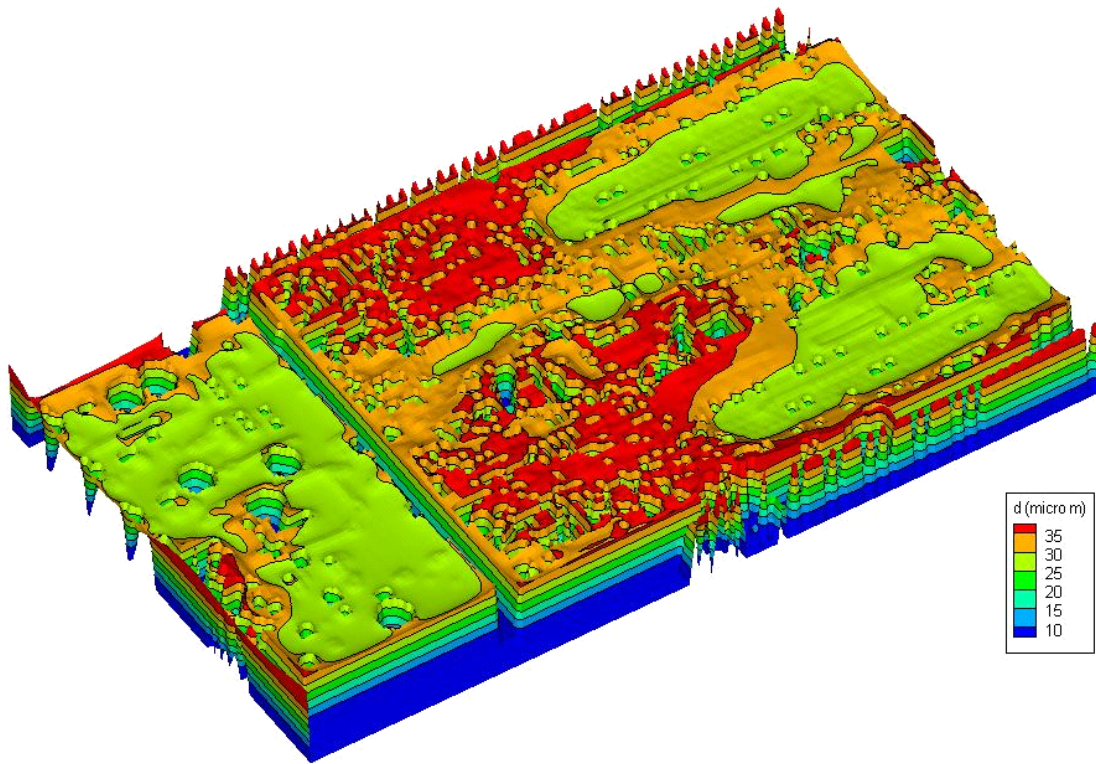


Figure 5: current density distribution (high values are in blue, red corresponds to masked areas)



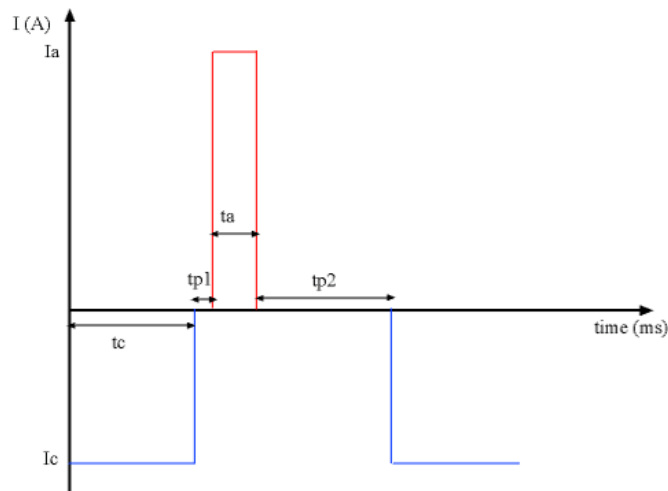
**Figure 6: copper layer thickness distribution in micron (high deposit thickness regions in red)**

Figure 6 shows the copper deposit layer thickness resulting from the calculations. Again the very high edge built-up is visible, especially for isolated features. Based on these calculations, improvements to the plating process can be determined.

To gain more insight in the plating processes on the micro scale (through holes, vias, ...), simulations need to be performed using more elaborate models. These models include the fluid flow, mass transport and detailed reaction mechanisms (both chemical and electrochemical) in order to generate accurate simulation results of the layer thickness distributions. Results from through-hole plating simulations using these extended models can be found for example in papers [3, 4] but are beyond the scope of this paper.

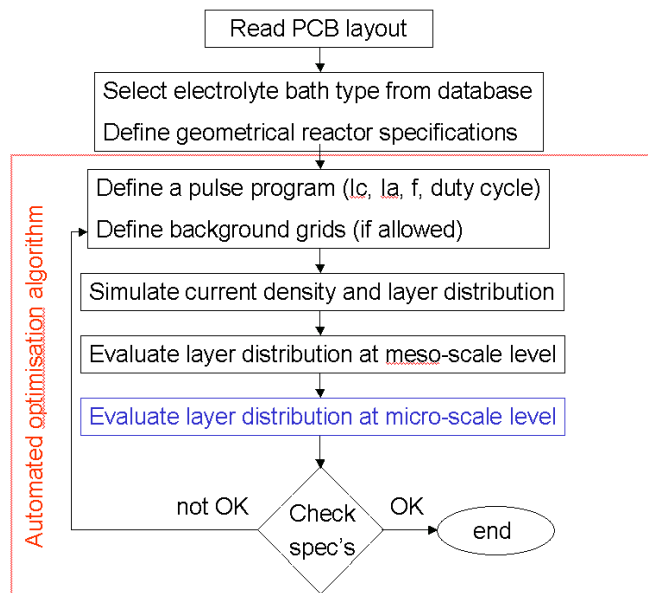
### **The P2ST Concept**

Macro scale current density distribution problems are mainly due to improper plating tank configuration, e.g. empty anode baskets, partly dissolved anodes, an ill-defined PCB rack configuration etc., as shown in the examples presented in Figures 1 and 2. But these problems can be solved relatively easily, and are of inferior importance to the meso scale current density distribution problems.



**Figure 7: bipolar pulsed current signal**

The performance of the plating simulation tool (P2ST) focuses on the meso scale level, while capturing also part of the macro scale effects. The concept is given in the flow chart of Figure 8. First, the circuit layout has to be read from some proprietary or standard file format (e.g. Gerber). Next the electrolyte bath characteristics for a specified acid copper type bath are retrieved from the available electrolyte database. Also the most relevant reactor configuration dimensions need to be defined (distance of boards to anodes, distance from one board to the next, etc.). Finally the Bipolar Pulse parameters (anodic and cathodic pulse height, anodic and cathodic on-time, off-time) as shown in Figure 7 or the DC current amplitude is to be specified in order to complete the required set of simulation input data. It's also possible to configure and specify an on-board thieving grid. Next the layer thickness distribution on the PCB is computed, and the result is compared to specifications (minimum and maximum allowed Cu layer thickness). The results of the simulation also give indications on the local micro scale plating performance (i.e. especially in blind and through-holes) through more detailed calculations or an expert system. If specifications are not met, the layer thickness distribution is computed for another pulse program. In a first release (v1.0) of the P2ST tool, the user has to specify by hand the pulse program for each simulation run. In later releases, an automated optimization algorithm will be implemented on top of the simulations, and the optimal pulse plating program will be delivered by the P2ST tool.



**Figure 8: P2ST operational flow chart**

## Conclusion

A performance plating simulation tool (P2ST) for the prediction of layer thickness distributions over PCBs and optimization of the pulse parameters has been presented. The focus is on meso-scale current density distribution problems (i.e. non-uniform layer thickness distribution caused by the circuit layout). Macro scale (reactor) parameters are also partly included, and a link to micro scale level layer thickness distributions is established.

## References

1. Purcar M., Van den Bossche B., Bortels L., Deconinck J., Nelissen G., Three-Dimensional Current Density Distribution Simulations for a Resistive Patterned Wafer, Journal of the Electrochemical Society, September 2004.
2. Choi Y.S., Kang T., Journal of the Electrochemical Society, 143 (1996) 480.
3. Chan S.H., Cheh H.Y., Journal of Applied Electrochemistry, 31 (2001) 605.
4. G. Floridor, B. Van den Bossche, L. Bortels, J. Deconinck, G Nelissen, 'DC and reverse pulse potential multi-ion simulations for a through-hole plating process, submitted for publication in Journal of Applied Electrochemistry