

“It is vanity to do with more that which can be done with less.”  
~ William of Occam

## **Robust, Simplified and Solder-Free Assembly Processing of Electronics Products**

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### **Executive Summary**

This white paper describes a new solder-free electronics assembly process tentatively being called *THE OCCAM PROCESS* in honor of the 14<sup>th</sup> century English philosopher and logician whose words inspired the concepts found herein. Products built by this process are expected to be more reliable than previous solder-free strategies (e.g., using conductive adhesive as a solder substitute) as well as traditionally manufactured soldered assemblies. The process is a reverse order interconnection solution that employs mature, low-risk, familiar core processing technologies in a novel sequence. Components are interconnected by means of copper plating after they are assembled into their final positions in an encapsulated module, thus doing away with conventional printed circuit boards. Prototype assemblies using this new technology are currently being characterized. The process is eminently suited to the manufacture of high-density, high-performance, high-reliability and environmentally (i.e., RoHS) compliant next-generation solutions for products ranging from consumer to military and aerospace applications. This process inherently eliminates high-temperature exposure, tin whisker risk, and vulnerability to mechanical shock and thermal cycle fatigue failure. Other anticipated benefits include simplified design (tightened geometries for higher density form factors), fewer processes (including elimination of all solder processing and associated issues), and diminished material costs and supply infrastructure.

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### **Introduction**

The technology described in this white paper addresses three serious challenges to producing electronic assemblies.

1. The regulatory imperatives (e.g., RoHS) to produce lead-free electronics requires subjecting them to very high temperatures associated with lead-free solder, and involves reliability risks associated with the extensive use of tin plating as a termination finish.
2. The relentless drive to reduce size and cost results in increasing challenges for reliable component placement and attachment.
3. Global sourcing and supply-chain expansion means more distant PCB suppliers, reducing the resources and support for domestic technology development.

An assembly designed and built using Verdant’s proposed reverse order interconnection process solution contains no solder. It, thus, completely bypasses the issues related to:

- The high temperatures required for lead-free soldering
- Flux removal from tiny spaces where it is not easily removed
- Mechanical shock and thermal cycling reliability of solder connections.

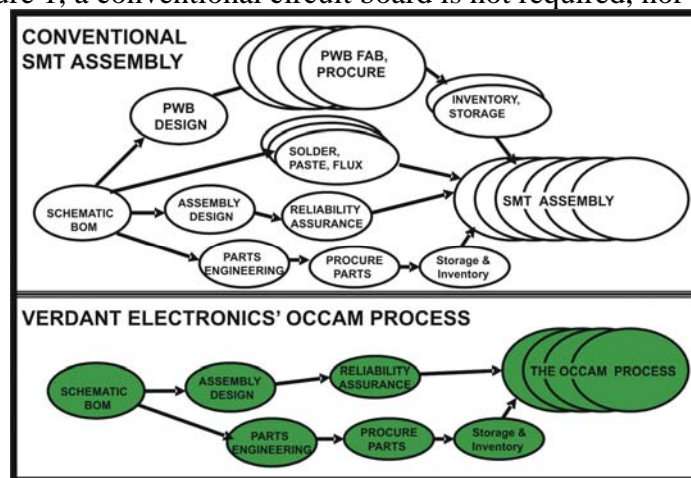
See Appendix A for a further analysis.

The assembly's fully tested and burned-in packaged IC components are pre-encapsulated. Encapsulation completely bypasses the issue of whisker risk due to the presence of tin plating on component terminations. It also eliminates any concern about complete coverage by conformal coating (for which there is now no need).

Though some embodiments of the technology can be used with traditional circuit boards, the more attractive assembly embodiments do not require a separately fabricated printed circuit board. It thus completely bypasses many of the issues related to supply chain management, inventory management, and design modification. Instead, the connections to the component terminations are created by copper plating to the exposed surfaces of the terminations arrayed across the encapsulated module's surface, with circuit layers created by either co-laminating or as has been done in the production of some bare die multi-chip and microprocessor modules in past years, the building up successive layers of circuitry. The interconnections can be redesigned as needed up to the moment they are made. Connections between layers are made during either the build-up or co-lamination, so there is no high-aspect-ratio via drilling. These assemblies are expected to be low cost and amenable to in-place thermal enhancements, EMI shielding, embedded electrical and optical components, and more.

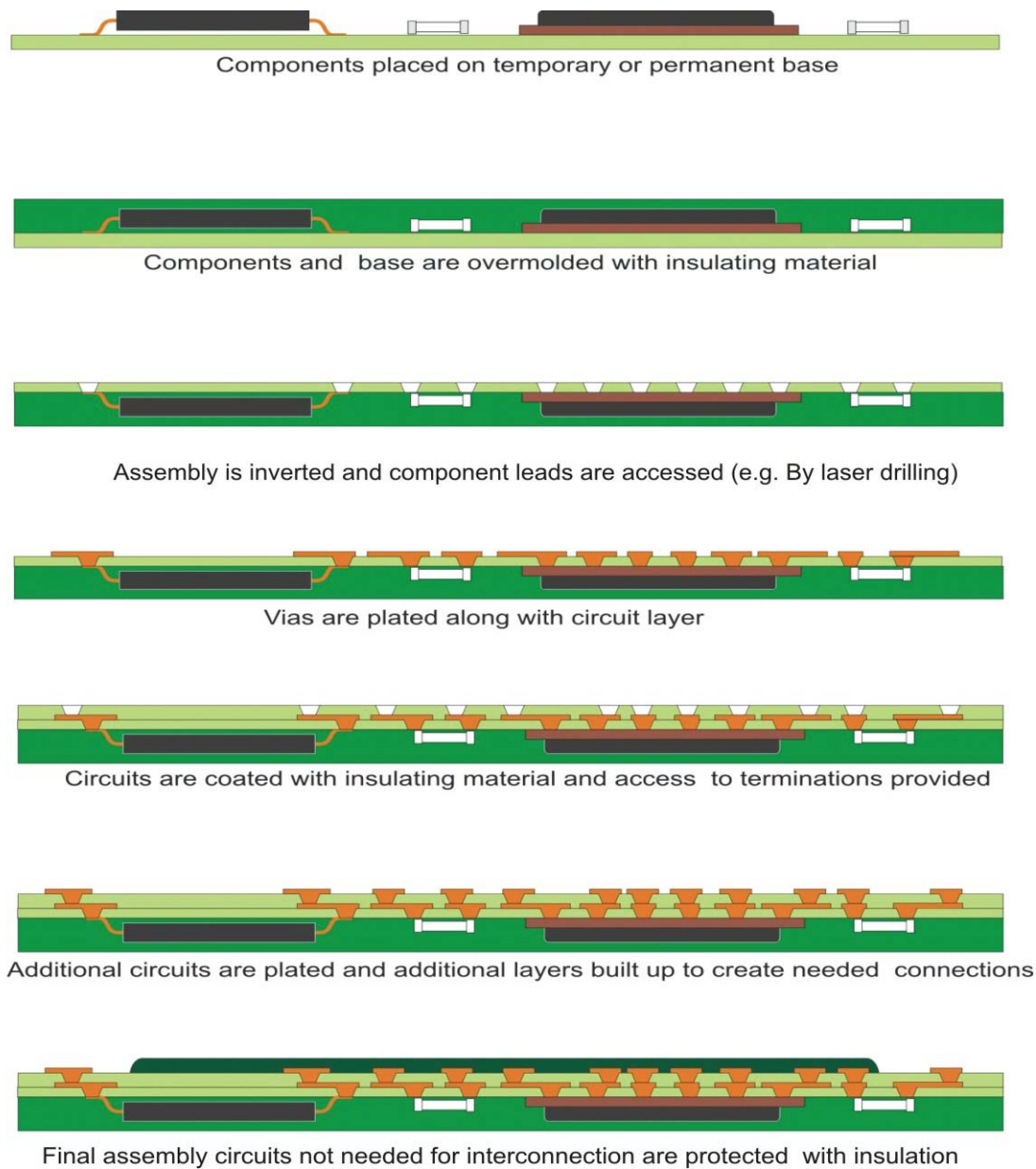
### Process overview

The Occam process is a reverse order interconnection process that employs mature, low-risk, familiar core processing technologies in a proven sequence. Components are interconnected by copper plating after they are assembled into their final positions. As illustrated in Figure 1, a conventional circuit board is not required, nor is solder.



**Figure 1** Graphic comparison of conventional SMT processing and the new approach. Note the implicit compression of supply chain and manufacturing cycle time.

In the build-up approach the conventional sequence of creating the interconnecting pattern between termination points (board fabrication), assembly and connection is reversed so that the sequence is simply assembly then interconnection.



**Figure 2** Basic process for a single component layer construction. Secondary operations and various enhancement options are not shown.

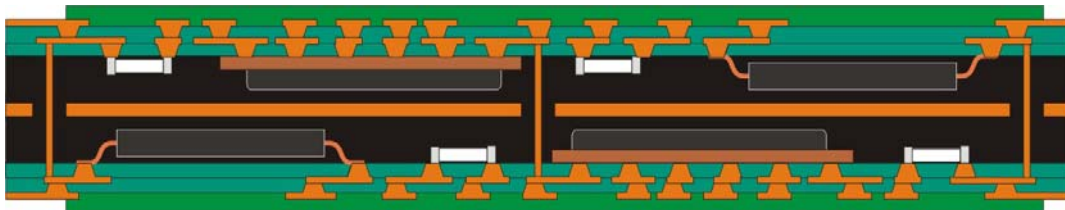
For purposes of comparison, in conventional electronic assembly, components are placed on board lands and temporarily immobilized by the contact between the terminations and pre-deposited solder paste until the solder is reflowed to provide the permanent immobilization. In the present process, components are placed on a removable tacky film on a temporary or permanent base. The film and base temporarily immobilize them until the structure is encapsulated. The entire array of tested and burned-in components

thereby becomes a monolithic assembly, with each component now permanently immobilized by every part of it. The bottoms of these terminations can be exposed by removing the temporary base and film or by making holes in a permanent one by such means as mechanical abrasion, water-jet material removal, or laser ablation.

The assembly is now ready to be metallized with copper using standard printed circuit additive (build-up) processing methods, with circuit patterns created to make the required interconnections between leads of all of the components. In most cases, more than one layer will be required, so an insulation layer is placed over it and the process is repeated until all required interconnections are made. See Appendix C for views of prototypes.

The final circuit layer can be connected to whatever user interfaces, displays and power connections are required for operation, and then coated with a conformal or rigid protective insulator layer. Where two layers of components are required they can be stacked and joined back-to-back with a central support, which could include various heat spreader constructions.

Figure 3 provides an example of a more advanced structure. Stacking and interconnection of assemblies from one side to the other can be accomplished by interconnection pins inside the assembly either individually as shown or in arrays. Interconnection between sides can be augmented by various connector structures or flex circuits as well. Note that these graphics do not show any of the thermal-management, optical interconnect, EMI, connector, 2nd-side, and odd-form enhancements that are enabled by this process.



**Figure 3** Stacking and interconnection of assemblies from side to side can be accomplished by interconnection pins inside the assembly either individually as shown or in arrays. Interconnection from side to side can be augmented by various connector structures or flex circuits.

## Discussion

Verdant Electronics' nontraditional concept involves the elimination of solder from the assembly process. The notion of eliminating solder is not new, but the previously proposed means to do so (e.g., replace with conductive adhesive) have not been accepted by the market, presumably because of difficulties in operation or lack of reliability.

While Verdant's solution is likely to be viewed early on by some as impractical at first because solder has always been the de facto standard for electronic assembly, those skilled in the technology of electronic assembly will recognize that is both possible and practical in view of the prior work in building much more complex and challenging multichip modules and IC packages using bare die. All of the materials, equipment and processes required to implement the process are available and operational today. The

biggest change to the assembly factory will be simply the importing of a mature process of additive board fabrication.

Because the process does not entail exposure of the assembly to the high temperature needed for reflow soldering, component moisture sensitivity level (MSL)--which is a measure of the risk of component damage due to explosive outgassing of absorbed moisture in the package during soldering--ceases to be a concern. All components can be treated as if they were MSL-1, which means that they do not require dry storage, special handling or recordkeeping. The process also allows use of components that are not capable of withstanding lead-free soldering temperatures (aluminum electrolytic capacitors, optoelectronic devices, connectors, etc.)

As with a standard printed wiring board, the interconnect structure still must be designed and fabricated, but some of the constraints are relaxed. There is no need for large component pads or lands for soldering, simplifying routing (see Appendix D). This allows a higher circuit density and hence a reduction in the number of layers needed. There is no need for drilling high-aspect-ratio vias all the way through the assembly as special structures have been anticipated to address the need when faced.

Also, eliminating the printed circuit board avoids many of the less obvious costs such as supply-chain management (vendor qualification, lead-times, incoming QC, etc.), testing, inventory management, protective storage, bake-out, handling, etc. Because the interconnection is not created until after assembly, the design can be modified as needed with no need for drills, fills and jumper wires. It is anticipated that the finished product will be totally encapsulated with a tough and properly CTE-matched epoxy or other material and, hence, be quite rugged.

In sum, the improved approach to assembly offers the OEM a new choice for producing products that should prove a highly reliable and cost effective approach to electronic assembly, while, as an added benefit, the products will not only comply with RoHS requirements but will actually be far more environmentally friendly than solder-assembled products. See Appendix B for a tabulated summary of process and product benefits of the Occam Process.

## **Development, qualification, and adoption**

Work is currently underway to develop the Occam Process from end to end. For example, several technical process and materials issues, workmanship attributes, inspection protocols, etc, associated with optimized and tailored interconnection options, need to be resolved, and are currently under development and investigation. These include:

- Refined definition of the encapsulant and its properties, particularly its shrinkage and CTE.
- Refinement of the manufacturing preparation steps: planarization, metallization, pretreatments, cleaning, etc.

- Refinement of the placement/positioning process, exploring the use of fiducials and true-position feedback.
- Refinement of the process to expose the terminations after encapsulation.
- Refinement of the build-up interconnection steps, including tailoring of the materials and processes.

Full qualification of the process and product will obviously be required but it is anticipated that there will be a number of willing participants among military product developers. Military suppliers and customers have been profoundly impacted by the wholesale move to lead-free electronics. Though they themselves are exempt from legislated lead-free requirements, military product developers are finding themselves increasingly unable to procure components with the tin-lead solder finishes that they know are reliable. See also the discussion in answer to Question 18 below.

Because solder joints are known as one of the “Achilles’ heels” of electronic assemblies, their elimination--enabled by the improved manufacturing technology--will cause high-reliability electronics product developers to want to evaluate it promptly. If it surpasses traditional assembly methods in terms of reliability alone, they should rapidly adopt the approach.

## **Business Considerations**

Verdant management is acting along a dual path.

- 1) **Technical** Development of testable, fully-functional assemblies using tested and burned-in packaged IC components and discrete devices, to continue and accelerate performance and reliability testing is underway. These assemblies will provide increasingly complex circuitry and performance, subjected to harsher and more in-depth protocols as well as regimens directed to MIL-aero qualifications. Testing will include electrical performance under humidity, temperature resistance, thermal cycling, solvent resistance, and vibration/shock performance. Further, process development using DOEs, or equivalent (as appropriate) is being planned, to define process targets and limits, materials characteristics, and QC/workmanship attributes and acceptance thresholds.
- 2) **Business** Arrangement of partnerships with appropriate entities including those with allied or related technologies, in associated test, materials, equipment assembly, and product development/OEM firms, to create and qualify specific product assemblies. The intent is to demonstrate functionality and reliability to suit target product applications, as well as to create specimens for industry distribution for broad-based testing.

The process has been reduced to practice on a small scale using tested and burned-in IC components, and prototypes are being created and characterized (see Appendix C). While patent coverage action is underway for various attributes and structures the company seeks to work cooperatively with other like-minded firms to offer benefit to the industry.

The necessary process development work to establish materials and process targets and tolerance boundaries, as well as to create testable assemblies for qualification, is being planned.

In today's manufacturing environment, to be qualified and accepted, any process must be available from more than one supplier. Verdant realizes this, and will be receptive to licensing and cross licensing of its own and others technologies for two good reasons:

1. Business opportunities are attractive for all participants.
2. Equally important, the technology will offer the most environmentally friendly electronics available.

Dedicated to serving the needs of both the electronics industry and the environment, Verdant Electronics' management holds to the premise that it is possible to "do well, by doing good."

The terms for deployment have not yet been established but with those guiding principles, favorable arrangements can be anticipated. See also the discussion in answer to Question 8 below.

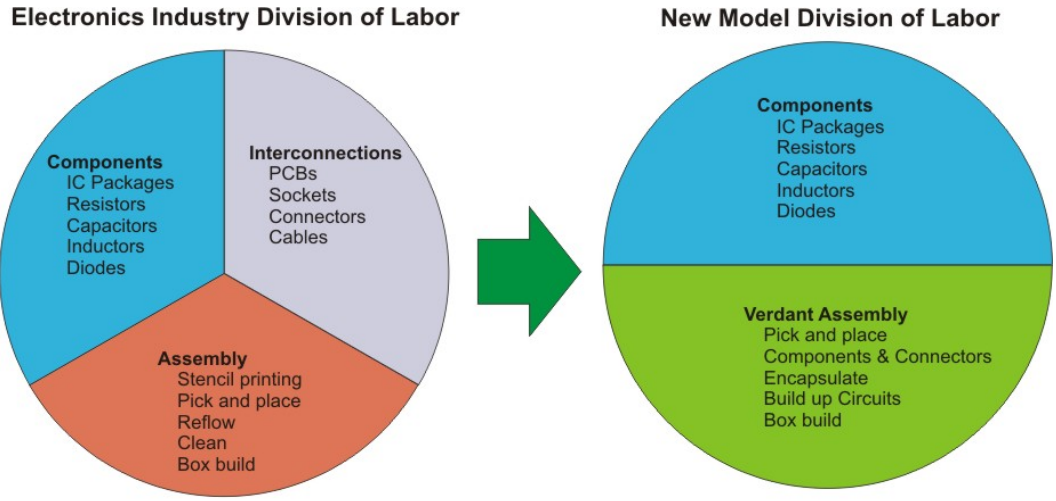
Verdant is in discussions with targeted partners and is actively searching out others to facilitate rapid and relevant development and qualification information. While no technology can be introduced overnight, it should not be difficult to implement either the present or future proposed solutions.

The technology has far-reaching implications. Instead of three different sectors for electronic manufacturing--PCB fabrication, components manufacturing, and assembly--there are just two (see Figs. 1 and 4). That is because printed circuit manufacture and assembly are essentially fused into one continuous manufacturing operation.

Such a solution will greatly increase control, and harness the revenue presently lost in supply chain management. A major [electronics supply chain management association](#) has stated:

"Billions of dollars in inefficiencies exist in the extended supply chain which few if any companies are able to identify, manage and capture on their own. This enormous value remains trapped up and down the chain and unlocking it would release billions of dollars to the ecosystem."

The technology greatly simplifies supply chain management by reducing to a minimum the number of items that must be managed.



**Figure 4** The proposed solution reduces industry fragmentation and shortens supply chain and cycle time

The technology could have a significant impact in the area of military electronics as well. As evidence are the words of a well known and widely respected researcher<sup>1</sup> from a military products company on the subject of RoHS:

As for problems brought on by RoHS, for those companies such as ours that build equipment not covered by RoHS, the biggest impacts are:

- Risk of tin whiskers on component terminations – on components bought and built into our equipment, and components built into dual-use COTS (commercial off the shelf) equipment we include in our equipment – due to the presence of lead-free tin plating. (Our mitigation strategy is to require the use of conformal coating on assemblies, with the assumption that there will be lead-free tin.)
- Prospect of non-availability of components we need that are not available with any finish other than lead-free tin. (Our mitigation strategy is to require designers to submit a non-standard part request explaining why the part is needed and assessing the whisker risk.)
- Lack of backwards compatibility of SAC BGAs – i.e., with tin-lead solder.
- Prospect of non-availability of BGAs we need with tin-lead solder balls.
- Prospect of receiving and accepting of SAC BGAs – due to our error or our supplier’s error.
- Prospect of someone in our organization signing a contract to deliver lead-free equipment without understanding the enormous implications.

Considering this list of concerns, it is evident that there is need to find and evaluate any promising solution that might mitigate such concerns at any level. This new technology,

<sup>1</sup> Gordon Davy, Northrop Grumman Electronic Systems, posted to the IPC Leadfree email forum.



targeted at the macro level problems of the electronic assembly industry, has the potential to address them all.

If broadly adopted by OEMs seeking to create less expensive, more reliable, and also more environmentally friendly electronic products, the resultant products could ultimately have significant impact on several business segments. Here are some examples (see also the discussion in answer to Question 13 below):

- The electronic solder industry, along with associated providers of flux, cleaners, stencils, etc., will feel the reduced demand.
- The EMS industry will adopt the technology to meet OEM demand.
- The conventional PCB fabrication industry and its laminate suppliers could decline over time as demand for conventional PCBs is displaced by new assembly capability.
- The tin industry, supported by global surface-mining enterprises, will be negatively impacted to the extent that tin is used to make solder for electronics. In the opinion of many knowledgeable environmentalists, a reduction in the use of tin solders for electronics is very desirable because it reduces mining and the energy of refining and soldering.

On the upside, the environment will benefit and so will the suppliers and consumers of high functionality electronics, particularly those seeking to make and buy products and applications that are mechanically robust, highly reliable and environmentally friendly.

See the Q & A section below for more in-depth discussions.

### **Benefits Summary**

The benefits of the proposed technology compared to conventional SMT technology, arise from several fundamental differences:

**No solder required or needed** – the Occam Process eliminates all the well-known and troublesome issues associated with SMT solder joints. See Appendix A for a view of the workmanship / design issues associated with any solder joint. More immediately, sidestepping the lead-free issue is a major additional bonus. The global electronics manufacturing services industry is approximately 115 billion dollars annually and has been reeling from the EU RoHS legislation.

The cost of lead-free solder assembly (preparation, yields, energy, reliability) is significantly greater than for traditional tin-lead solder assembly. This impacts the bottom line of the EMS provider and the OEM. The new approach offers the OEM a new choice for producing products that not only comply with RoHS requirements but which are truly more environmentally friendly and, moreover, should prove to also be the most reliable and cost effective approach to electronic assembly yet devised.

Perhaps most important is the fact that the technology can be implemented almost immediately. All of the materials, equipment and processes required to implement the technology are available and operational today. Appendix E provides a long list of benefits. Certainly avoiding costs of all solder materials as well as capital processing equipment will be a substantial benefit but so also is there significant potential for energy savings--perhaps 2 to 3 billion kWh per year by the elimination of the solder reflow process and baking equipment. In the USA the average cost per kWh is approximately 10 cents so the savings potential is significant.

Note that lead-free brings with it a series of "green" PCB requirements, impacting not just finishes, but also internal PCB construction materials. The improved technology renders all that moot. Another bonus arises from the new approach's benign thermal conditions, in contrast to the high-temperature excursions to 250°-270°C required for lead-free assembly. Thus, all components default to MSL-1 (moisture sensitivity level 1, the lowest level of concern where no pre-baking of components is required prior to assembly). This new low-temperature processing enables use of conventional inks, sleeves, wires, coatings, standoffs, connector bodies, etc

**No PCB required** - Eliminating the printed circuit board circumvents the whole spectrum of circuit-board challenges and costs, including PCB design, supply-chain infrastructure (vendor qualification, lead-times, incoming QC, etc), testing, inventory, protective storage, bake-out, handling, etc. It is recognized that, while traditional PCB fabrication is eliminated, some of the equivalent elements must be put in place to provide the build-up process. This will be a substantial task, but one which requires no discovery or invention because such processes are well-known and understood today. Moreover there are alternative embodiments of the technology in development which can bridge the transition period.

**Total encapsulation** - The finished product will be totally encapsulated with a tough epoxy or other material, properly CTE-tailored, with proper internal adhesion-appropriate mechanical and electrical properties, short- and long-term reliability. It is expected to be exceedingly robust. Further, depending on enhancements, desired thermal, ESD, EMI, and barrier properties can be achieved. See Appendix C for views of prototypes.

**Ease of design and circuit routing** - Direct copper-to-copper build-up technology does not require the large internal circuit capture lands required in conventional circuit-board construction, freeing up significant real estate for additional circuit routing and a reduction in layers. Therefore, much higher density circuitry can be achieved and, at the same time, layer count can be reduced. See Appendix D for examples of routing advantages.

## Questions and Answers

- 1) **Build-up technologies require very high yields at each step. Is the technology mature enough to risk entire assemblies?**

**Answer:** Yes. [Build-up technology](#), used in substrate fabrication and the creation of high density interconnect (HDI) IC packages, is very mature. Moreover, some of the concepts being proposed for creating solderless electronic assemblies of tested and burned-in IC packages are used in the creation of IC packages themselves; plated contacts are made to terminals on the unprotected IC, which are often of unknown or uncertain quality. These IC package assemblies pass high-temperature soldering requirements when soldered to the board. This provides heritage evidence that the process, as applied to Level-2 assembly, should provide adequate reliability. With the new interconnection approach the yield should be equivalent to or even better than IC packaging yield, which is much better than solder joint yield. The feature sizes and material set and robustness of interconnection interfaces makes it possible to produce highly reliable products.

**2) Are materials available that are suitable for encapsulation? Have any materials been qualified?**

**Answer:** Yes. Several off-the-shelf [materials](#) appear suitable. Requirements for encapsulants include dimensional stability, resist excessive shrinkage resistance, good insulation, low moisture uptake and outgassing, and having a CTE approximating the CTE of common components (e.g., copper  $\sim 18\text{ppm}/^\circ\text{C}$ ), plus all the appropriate mechanical properties. Material developers have a long history of producing such products. It is anticipated that this target property balance will be feasible. Qualification depends on the application, but coatings and potting materials tailored for successful harsh MIL-aero and under-the-hood applications have been available for years. No problems are anticipated in finding and demonstrating suitable solutions.

**3) Can the improved technology accommodate all types of SMT packages?**

**Answer:** Yes. Early prototypes were created using a range of components, various QFPs, TSOPs and QFNs (see Appendix C photos). A second prototype was produced using BGAs, which were planarized to become LGAs. An attractive feature of Verdant's improved approach is its suitability for the LGA and QFN packages. These are attractive from a design perspective (high performance and high density), but are also most prone to opens and solder-ball shorts because of constrained solder-joint geometry and difficulty of inspection. The technology enables more separation to minimize shorts and/or additional routing clearance and topology. Verdant will work closely with package developers to define the types of package that will work best. A Southern California startup, [Mirror Semiconductor](#), is developing a concept for IC packaging that will very likely be able to take synergistic advantage of the concepts proposed herein. The technology is also favorable for use with the advanced IC packaging concepts disclosed by [SiliconPipe, Inc.](#) That company's OTT (Over or Off the Top) and SSP (Stair Step Package) concepts offer highest performance as well as lowest cost options available today. The new solution enables and is readily adaptable to interconnection of these cost-effective, high-performance package technologies.

**4) How critical is IC package lead coplanarity?**

**Answer:** Coplanarity is important but it is not a “show stopper.” Several lead conditioning options within the technology are available; the process using laser drill feature access should accommodate any small variation in lead heights. Note that all the conventional solder-joint problems encountered in conventional SMT processing (placement, solder-gap, tomb-stoning, pad-land match, registration, starving / excess solder, voiding, cold/disturbed, etc) are non-existent in the improved technology.

**5) ESD is a growing concern; can the technology provide solutions?**

**Answer:** The answer is yes. Emerging technologies for ESD protection appear to be well-suited to circuit protection. A leading company in ESD technology is [Electronic Polymers, Inc.](#) A cooperative relationship between EPI and Verdant and technologies is expected to yield the most ESD-immune product technology on the market today.

**6) Have other solderless possibilities been explored?**

**Answer:** Yes. Alternatives have been discussed for many years, with essentially no success to date. Uni-ax elastomeric connectors showed some niche promise but had difficulties. Conductive adhesives serve limited tasks of development, cuts-and jumps and breadboarding. In every case, however, solder has remained the process of record and interconnection to a separate printed circuit was required.

**7) Can the improved technology offer thermal management solutions?**

**Answer:** Yes. This technology appears ideally suited for thermal management options. Heat spreaders, phase-change systems, heat-sinks, and even heat pipes can be placed directly on top of or between components prior to assembly and will become a part of the assembly itself. This is because there is no concern about getting cold solder joints as would be the case for standard processing. Many prospective solutions (such as integration of a heat spreader) can be designed-in early in parts engineering to take advantage of placement and proximity potential with the improved approach. Similarly, it is anticipated that the component package itself can be optimized (i.e., to bypass the solder ball placement step). Further, advanced materials development is proceeding elsewhere that will offer electrically-insulating encapsulants that also have high thermal conductivity, possibly enabling other thermal-management solutions.

**8) Will multiple sources of the technology be available?**

**Answer:** Yes, that is anticipated. In today’s manufacturing environment, to be qualified and accepted, any process must be available from more than one supplier. Verdant realizes this, and encourages licensing for two good reasons: business

opportunities are attractive, as discussed above, and, equally important, because the technology will offer the most environmentally-friendly electronics available. Dedicated to serving the needs of both the electronics industry and the environment, Verdant Electronics' management holds to the premise that it is possible to "do well, by doing good." The terms of licensing have not yet been established but with those guiding principles, favorable arrangements can be anticipated.

Presently the company is working with a progressive, multiply-capable electronic manufacturing services company, [Promex Industries](#), in Santa Clara, Calif., where early development is taking place. Lessons learned are being collected and codified for transfer to future licensees/users. Promex, with its experienced team of engineers and technicians, will be the vanguard company in helping to produce early generation products using Verdant Electronics' improved methods.

**9) Isn't this too "blue-sky"? Doesn't the technology require lots of invention and discovery before it can achieve commercial reality?**

**Answer:** No. Based on decades of electronics assembly manufacturing experience, product configurations are well known, the core processes are well-known, failure modes are well known, fabrication processes and capabilities are well known. Materials and product reliability and QC protocols, etc., are well known. Peripheral support resources (cleaning, conditioning, lab analysis, etc.) are available.

**10) This looks a bit like some earlier IC packaging technologies. What's the difference?**

**Answer:** In the 1990s, an innovative team of engineers and scientists at GE created multichip modules packages using blind vias and build up circuit technologies to interconnect them. Others have followed that lead including Intel with its BBUL microprocessor chip and universities and technical institutes in Europe. Researchers in Japan have also been working on buried active device assembly. In every known case, the developers are working with bare IC die and not tested and burned-in IC packages. The problem with bare die is twofold: 1) The entire assembly must be completed and burned in before the yield of the die is known and this has hampered broader scale use; 2) Bare die is nonstandard in terms of both size and pin out making design a challenge as a library of registered components is virtually impossible to obtain. Another difference is that almost all modules created in this fashion were designed to be assembled to printed circuit boards and most often with solder. In short, known prior efforts have been primarily on building micro electronics using microvias in an IC fab-like environment and the improved technology will be focused on assembly macro electronics and interconnection *macrovias* produced in printed circuit shop environments with no solder in the final assembly.

The new concept also differs from known prior work in that it proposes to have components back to back with through connections where required to make side-to-side connections and the stacking and lateral interconnection of assemblies. There are

a number of other innovations and improvements in the works as well to advance the concept.

To reiterate and summarize, a key difference between earlier and presently developing concepts and the processes in development is that robust, tested and burned-in IC packages will be used in place of the delicate and bare silicon chip of uncertain quality. In recent years embedded passive and embedded active (i.e., IC chip) modules and PCBs have been described but these modules and PCBs are, so far as is known, still being designed to be soldered to a next-level assembly. The technology presently in development proposes the complete elimination of solder and all of the associated problems it brings with it. This is an important distinction in the evolutionary development of improved electronics over time where each succeeding generation builds on the foundations of earlier work. To paraphrase Isaac Newton: “If Verdant Electronics has been able to see a bit further than others, it is because it has benefited from standing on the shoulders of giants.”

**11) Will products built this way be Underwriters Laboratories (UL) certifiable?**

**Answer:** Indications are favorable, although no submittals have been made at the time of this writing. Verdant’s technology is a departure from the norm, but is expected to be produced using legacy materials that are [UL certified](#). Testing and information exchange is anticipated and acceptance is expected; especially because the improved process technology does not thermal-shock the electronics nor require high temperature exposure, typical of conventional SMT processing. Flame retardation will be important, and material-selection will accommodate that capability.

**11) Is the technology and structure appropriate for a variety of product types?**

**Answer:** The technology will be useful for a wide range of applications of volume and complexity; from low volume/low complexity to high volume/high complexity, thru low-volume, high-complexity, highest reliability products. The first areas of interest will include consumer products, memory modules, phone modules, computer card modules, RFID and smart cards; and high reliability electronics for military, aerospace, under-the-hood, and medical applications. Beyond these conventional applications, improved products are envisioned to succeed also in flexible circuits, and curved-substrate products. While the first functional prototypes are simple LED circuits, it is anticipated that cell phones and military products could be leading candidates for product qualification and introduction, given their demands for high-reliability, high-density, thermal and mechanical-shock resistance, especially in the face of the current lead-free imperatives. See Appendix C for examples.

**12) Is the technology appropriate for X-Ray inspection?**

**Answer** Yes, should it be necessary or simply desired for whatever reason. The encapsulant will not obscure the image, and subsequent build-up steps should be readily verifiable in-process because of fewer copper planes and traces.

**13) Will related industries be affected by this reverse order process technology?**

**Answer:** Yes. The technology could eventually have a significant impact. Solder for electronics is a ~ \$600 million annual market. This represents ~ 1% of the roughly 110 billion dollar EMS market. The effects will not be immediate, of course, because of the inertia of current manufacturing. The compelling advantages of Verdant's approach are expected to have far-reaching effects that will include the manufacture of reflow ovens, flux manufacture and cleaning equipment and chemistry suppliers. Further, the disruption and compensatory response of the PCB fabrication and support industry will be similarly significant but it also opens doors to new opportunities.

**14) Will the technology have any impact on the semiconductor industry?**

**Answer:** Yes, and beneficially, based on the benign nature of the processing and reduced thermal shock and profiles. The technology could have other bonus far-reaching impacts based on that same room temperature process potential. A range of prospective semiconductor materials have been identified and they are available to varying degrees. Some have reportedly been excluded from consideration because of the thermal excursions expected in assembly. It is possible that this new process could open the door to a broader range of prospective semiconductor materials. As an example, a clear benefit to the optoelectronics industry is likely, because their components could be used with the process, avoiding the high temperatures encountered in conventional solder assembly... especially now that lead-free processing is seen to require some reflow profiles that are approaching 260 °C.

**15) Will this technology have an impact on electronic product design?**

**Answer:** Yes. The solutions in development are expected to have a very positive effect on design, in that they have the ability to open routing channels and thus reduce layer count requirements. Moreover, the technology offers the designer the opportunity to completely ignore non-functional lands, thus opening up additional circuit real estate to prospective additional use in routing or spacing circuits. New products will likely arise to take advantage of improved thermal management, embedded components, physical structures, topology and mechanical-property options. Additional concepts are being collected and codified relative to design to allow for the creation of brick like assemblies that can be interconnected on all edges and both major surfaces. Moreover, the concept extends to the creation of interconnected brick-like elements that are interlaced with cooling features that have not been available before. Design and EDA tool developers have been made aware of the opportunity and it is anticipated that they will begin to modify their tools to meet the slightly different needs of the new technology and make the designer's job easier.

**16) Can the technology facilitate high-density designs?**

**Answer:** Absolutely. Using this reverse order process technology designs can be much higher-density, simply because surface catch-pads and non-functional internal via pads are eliminated, and routing topology can be optimized, and tolerance stacks will be tighter. (See Appendix D)

**17) Can products designed in this manner offer electromagnetic interference (EMI) protection?**

**Answer:** Yes. Improved designs can embody conductive elements (metallic coatings, screens, shields, etc.) locally or spanning and covering the entire assembly. The EMI metal-coat will thus block both the emission of and reception interference by EMI radiation. Moreover, with a metal coating, it could be nearly hermetic.

**18) How will the technology address the assembly of passives (chip-caps, chip resistors, MELFs, etc.) and other packages, whose terminals are typically tin-lead solder-plated?**

**Answer:** This is an important question and there is no definitive answer at this moment. While there is nothing intrinsic in solder that would inhibit a metal such as copper from being plated to tin, solder--whether tin-lead or lead free--is not plated to under normal circumstances. It is in fact very possible that the solder finish can be reliably activated and plated to but there is need to prove that such is the case. The most desirable finish for component package leads appears to be copper and this would obviate the need to overplate the leads, thus avoiding that expense.

Pre-treatment could offer solutions and further development may be necessary. However, because the interconnections will be encapsulated and not be as highly stressed, as are traditional soldered components, this may prove to be a non concern. As an option, until there is certainty that there is need for a new finish and it is broadly instituted by discrete component suppliers, discrete devices can either be integrated into the assembly and soldered to a component or they can be assembled to a carrier using conductive adhesives and processed as a regular component. Since a significant number of circuit failures are related to discrete devices' solder joints because of high temperatures, any of the methods described could significantly improve final yield.

It is expected that over time and initially in critical niches, a package supply segment will arise that will offer lower-cost copper end terminations, optimum for the technology.

**19) Can the technology accommodate very small geometries, such as with 0201 and 01005 discrete devices?**

**Answer:** Yes. Any device that can be handled and placed is useable. In fact, the shrink advantages with these tiny devices are more desirable, because large solder-



fillet lands are not necessary with the technology and overall density can thereby be increased.

**20) Can the technology deal with misregistration, at placement and then during encapsulation, should it occur?**

**Answer:** Yes. This is important. It is true that the familiar molten-film self-centering effect will not exist with the proposed process. As with conventional SMT processing, initial placement errors and damaged leads will be one of the improved technology's processing challenges. It is expected that these issues will be resolved using careful rheological and dispense control tack-films, smart optical pattern-recognition targeting, and/or adaptive point-point interconnect. In fact, it is expected that the improved process will prove superior, in that perfect coplanarity and positioning may not be required, in all situations, given the adaptive capability of subsequent plate-up steps.

**21) Are rework or second operation possible using the improved technology?**

**Answer:** Yes, but likely it will be with some difficulty. Fundamentally if it becomes necessary to rework, something must have gone unnecessarily wrong with the design and/or process. That said, concepts for rework have been considered. These could involve the removal or isolation of the defective parts (such as by laser or water jet cutting) and replacement with a new device. Circuit rework, "cuts-and-jumps", "white-wiring," etc., will be a similar processing challenge. It is conceptually possible to, in essence, erase the circuits and begin again. These process development and demo tasks are being planned. The preference is, of course, to design and build the structures right the first time.

**22) Can the technology accommodate present and future direct-write PWB concepts?**

**Answer:** Yes. Exploratory work confirms that direct-write could create the desirable interconnect integrity. Material selection, particularly conductivity and adhesion, will be key, enabled by the benign thermal profiles used in the improved process. Encapsulation of circuits and the lack of mechanical stress should ameliorate many concerns.

**22) Can the improved technology accommodate optoelectronics?**

**Answer:** Yes. It is anticipated that the technology will be adaptable for use in optoelectronic applications and the concept can be adapted to the integration of copper and photo optical channels for data transmission. It should be noted that the more benign lower-temperature process in development is more adaptable to thermally-vulnerable photonic and optoelectronic systems. Certain additional capabilities such as access / placement, positioning and alignment, transparency, etc.

could offer further advantages. The technology could help reinvigorate this optoelectronic industry, stalled since the collapse of 2001.

**23) Are there other possibilities for interconnection of the components beyond those just mentioned?**

**Answer:** Yes. Some of the technologies of earlier years could be resurrected for this technology. For example, stitch wire and resistance welding wire interconnection and laser welding methods are options for making point-to-point connections. Conceivably, wire bonding technology can be used to make desired connections. These discrete wire technologies offer very quick path solutions to one of a kind or low volume assembly. Also envisioned is the possibility of making coaxial connections between components as needed. Moreover, air dielectric constructions are a possible option for high-speed applications.

**24) Will the assemblies cost more?**

**Answer:** No. They should become less expensive because of fewer materials and process steps, less energy, shorter supply chains, fewer intermediate processors and, ultimately, much less material waste. Certainly better comparative data awaits more experience with actual products and high-volume runs, and development of support infrastructure, over time.

**25) What can be said about reliability of these assemblies?**

**Answer:** This is an extremely important question. No testing has been done yet, but reliability experts who have seen the concept have very positive expectations. The reduction in the number and type of interconnections is a big step in the right direction. As world renowned reliability expert Werner Engelmaier observes:

*“Page: 18*

*The big difference is that there are no connections subject to creep-fatigue, since nothing in this interconnection technology requires a low melting temperature, and thus operating temperatures will be way below a homologous temperature of  $T_h=0.5$  where creep becomes significant. The fatigue, to the extent it will occur, will be all in high-cycle fatigue, something just not possible with solders where all fatigue is low-cycle fatigue in combination with creep.”*

Elimination of all soldering issues, especially lead-free issues, is a key benefit. Actually, the reverse order processing concept eliminates all the industry-recognized solder-joint vulnerabilities. Conventional PCB plated-through-hole vias, as mentioned earlier, are most vulnerable to high temperature excursions. In contrast, because all electrical interconnections become solid monolithic, interface-free, and because

processing takes place at near room temperature, temperature induce risks are reduced. Certainly, these benefits must be demonstrated, tested, qualified and validated. These efforts are ongoing and planned.

**26) There are many different types of lead finishes presently used on components. Can they all be reliably plated to?**

**Answer:** The base metal on most components today is copper and it is possible to remove the finish to expose copper, which can be reliably plated to. This has been well demonstrated over the history of PCB technology. There are some Alloy 42 lead frame materials in use but mostly for ceramic packages. Plating processes and compensatory measures, within the improved process and/or upstream in packaging technologies will arise. Wholesale change is not expected to happen overnight. These solutions will be rolled out over time, along with support technologies and infrastructure. Logic and economics indicate that there should be only a limited number of package types and finishes in the future.

**27) What about connectors and sockets? Can they be added or connected to the assembly if needed?**

**Answer:** The body of the assembly can serve as an edge card connector if desired. This is much like a standard PCB assembly. On the other hand, discrete connectors and sockets are much like components and can be put in place like a component. They may require special preparation, such as protective caps, to shield and protect their contacts through processing and until they are ready for use. When ready, the protective cap can be removed and a solderless processor or other assembly can be socketed and/or the connector can be mated to its male or female counterpart. Certainly at any point the improved assembly can accommodate compliant-pin, press-fit and similar odd-form second-operation components. It is likely that many new types of connectors and sockets will be developed in the coming years to take advantage of the unusual capabilities and economies.

**28) This seems like a very large and daunting task. Even if the industry accepts the ideas, won't it take the industry a long time to adapt to this new way of manufacturing?**

**Answer:** There will be many challenges ahead, of course, but the fundamental ideas behind the proposed approach builds on the proven ideas of many different technologies of the past. Though invention and reinvention are part of what is being proposed, it is not so much a matter of invention as it is one of orchestration and bringing the right technologies into play in the right order.

As to the matter of how long it will take, that is a matter that will be determined by the collective will of the industry to change. Change always comes with or without our consent. The question companies must ask themselves is: "Do we want to be the master of change or do we want to be its servant?"

For inspiration in this matter, Verdant Electronics management has turned to the sage advice of the late 18<sup>th</sup> and early 19<sup>th</sup> century German philosopher, Johann Goethe who said:

*“The moment one definitely commits oneself, then providence moves too. All sorts of things occur to help one that would never otherwise have occurred.*

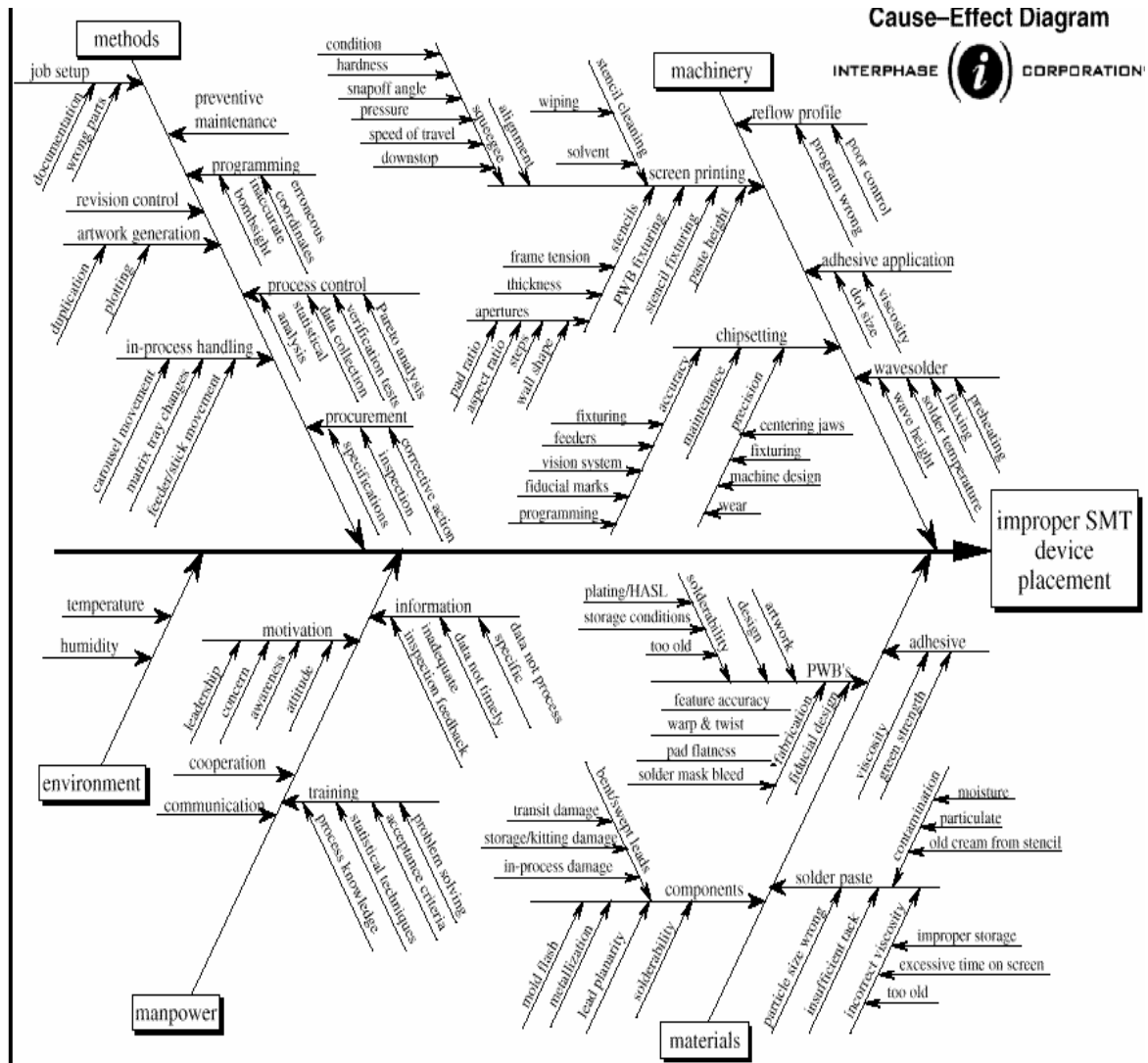
*A whole stream of events issues from the decisions, raising in one’s favor all manner of unforeseen incidents and meetings and material assistance which no man could have dreamed would have come his way.*

*Whatever you can do or dream you can, begin it. Boldness has genius, power and magic in it.*

*Begin it now.”*

*~Johann Wolfgang von Goethe*

**Appendix A Solder-Joint complexity.** Note all the factors leading to a properly placed solder-joint.

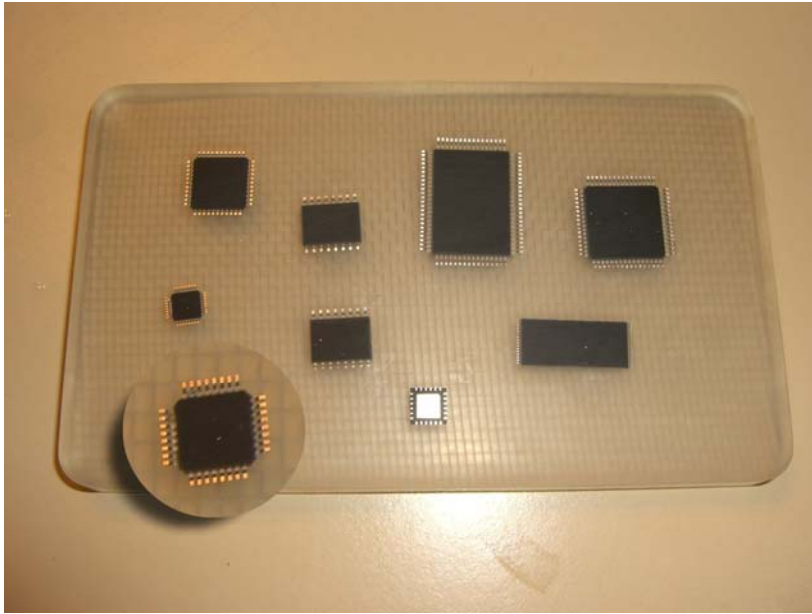


## Appendix B Benefits of Verdant Electronics' Occam Process

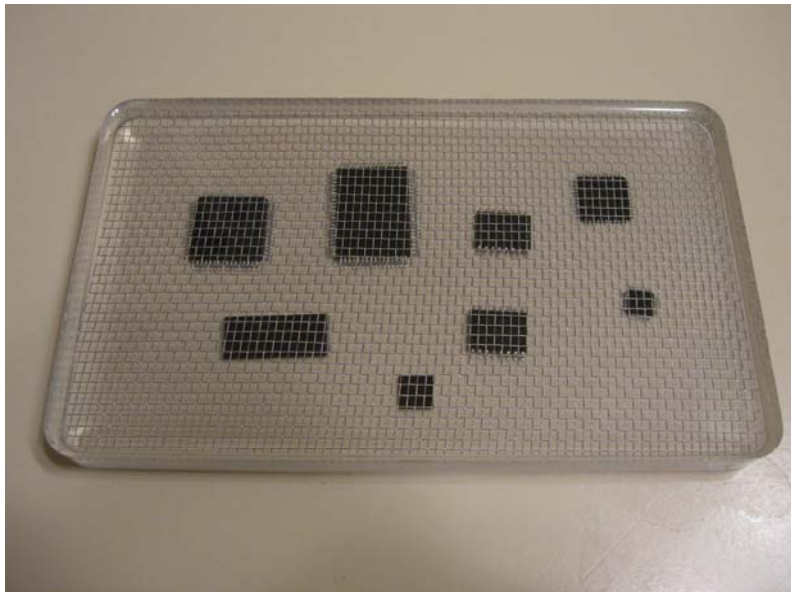
Primary benefit	Secondary Benefit
No PCBs required	<ol style="list-style-type: none"> <li>1) No PCB procurement</li> <li>2) No PCB testing required</li> <li>3) No spares required</li> <li>4) No finish or shelf life issues</li> <li>5) No board warpage concerns</li> <li>6) Completely additive with low material use and near zero waste</li> <li>7) All copper system (no special finish concerns)</li> <li>8) Integral connector constructions are still possible</li> </ol>
Elimination of soldering	<ol style="list-style-type: none"> <li>1) No RoHS restricted material concerns</li> <li>2) No board finish or component solderability concerns</li> <li>3) No solder inspection required (no solder shorts or opens)</li> <li>4) No high temperature damage</li> <li>5) No component and assembly moisture bake out required</li> <li>6) Significant energy use reduction by eliminating reflow</li> <li>7) Eliminates solder the weakest link in electronics assemblies</li> <li>8) No difficult cleaning required</li> <li>9) No post cleaning or cleaning residue concerns</li> <li>10) No solder reliability issues</li> <li>11) Reduced manufacturing steps</li> <li>12) Higher performance possible by elimination of solder discontinuities</li> <li>13) No tin whisker concerns</li> </ol>
Works with standard components but facilitates use of more efficient components	<ol style="list-style-type: none"> <li>1) No delicately shaped leads required on components</li> <li>2) Components more easily tested and burned in before assembly</li> <li>3) More robust processing possible with all leadless components of reduced types needed (e.g. QFN and LGA types only)</li> <li>4) Lower cost higher yield devices</li> <li>5) Can free routing space on area array IC packages</li> <li>6) Easier test socket designs</li> <li>7) No solder contamination of test contacts</li> <li>8) No MSL issues (e.g., No popcorning)</li> <li>9) Amenable to integration of embedded passives</li> <li>10) Amenable to use with integrated passive assemblies</li> <li>11) No solderability testing concerns</li> <li>12) No RoHS concerns</li> <li>13) Compatible with important advanced package and interconnection concepts (e.g. OTT, SSP)</li> </ol>
Improved Robustness	<ol style="list-style-type: none"> <li>1) Room temperature processing avoids thermal damage of soldering</li> <li>2) Components are fully encapsulated increasing shock and vibration immunity</li> <li>3) EMI protection can be made integral with 360° of metal protection</li> <li>4) Simple structure with fewer elements</li> <li>5) Integral heat spreader possible because soldering is not required</li> <li>6) Circuit side can be finished with a heat spreader if desired</li> </ol>
Greater design freedom	<ol style="list-style-type: none"> <li>1) Components can be placed closer together to conserve space</li> <li>2) Integral heat spreader allows for redefined placement rules</li> <li>3) Completed assemblies can be stacked and interconnected</li> <li>4) Can be readily adapted to optoelectronics</li> <li>5) Increased routing capability (no solder lands required when making circuits)</li> <li>6) "Dead" leads can be ignored freeing additional routing space</li> <li>7) Easy and low cost reconfiguration and ECOs</li> <li>8) Can be used for flexible circuits</li> </ol>
Testing and reworkability	<ol style="list-style-type: none"> <li>1) Assembled components can be functionally tested as an assembly before circuits are built up to facilitate trouble shooting if desired or needed</li> <li>2) Circuits can be "erased", components removed and reprocessed. The technology allows for mixtures of interconnection technologies to be integrated for ECOs if needed</li> </ol>
3D Stacked Assemblies	<ol style="list-style-type: none"> <li>1) Additional component layers can be added on top of each other or a layer can be added orthogonally to other layers or at other angles into one stacked assembly with interconnection layers between.</li> <li>2) Interconnections could go from any layer to any other layer not just to the adjacent component layer.</li> <li>3) Interconnections can be made accessible from all sides of the stacked assembly not just one or two sides.</li> <li>4) Interconnections can be stairstepped (via SiliconPipe technology).</li> <li>5) Heat spreaders can be added in between layers if required.</li> </ol>

## Appendix C

Pictures of early Proof-of-Concept modules



**Figure C-1** Initial process demonstration module, using various types of components with and without leads (insert shows copper terminations ready for connections).

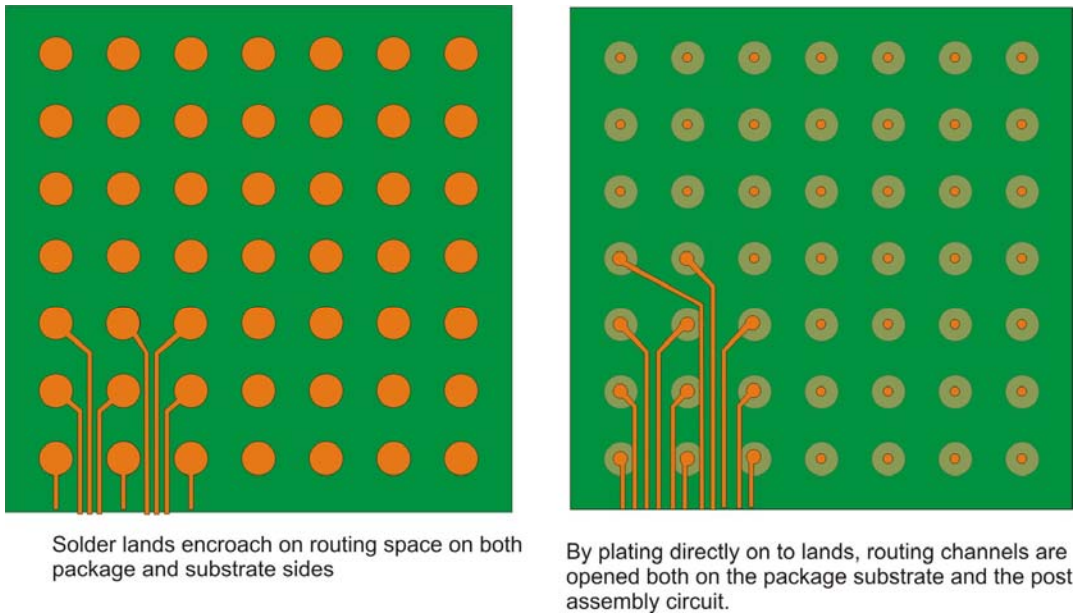


**Figure C-2** Backside view of the assembly showing an embedded metal screen for shielding or other purposes.

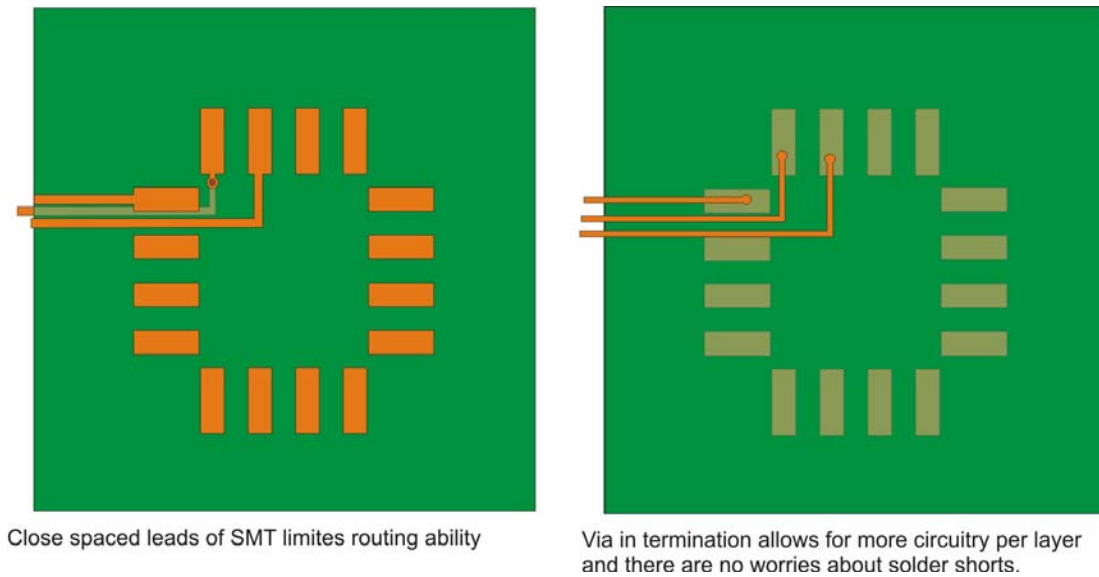
## Appendix D

### Between-the-elements routing benefit, enabling smaller internal features and higher densities

As indicated in Table 1, there are significant design benefits, including significant increases in routing channels and as well a reduction in layer count while eliminating all concerns over solder shorts and opens. This is visually depicted in Figures D-1 and D-2.



**Figure D-1** No via-in-pad concerns provides routing advantage for area array devices and a significant reduction in capacitance.



**Figure D-2** Routing advantage for QFN and similar peripherally leaded devices.